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42	BOM

IH11M-MHS H110MD PRO D4 VER 6.0

CPU:

Intel Skylake S 42 in LGA1151 Package 95W

System Chipset:

SPT-H PCH

Main Memory:

Dual Channel/DDR-4*2(Max 16GB)1867/2133

Onboard Device:

Super I/O:IT8613E

LAN:Realtek 8111H

HD Codec:ALC887

Power solution:

CPU Voltage Regulators:3phase by RT3606

high 1 Low 1 OV by RT3606

DDR Voltage Regulators:1Phase by UP1514

high 1 Low 1 OV by IT8613E

Expansion Slots:

PCI EXPRESS 16X SLOT *1

PCI EXPRESS 1X SLOT *2

REAR IO:

PS/2 PORT

DVI Port

VGA Port

USB3.0 PORT *2

Gb RJ-45 +2 layer USB3.0 Ports

Audio Jackets (3 PORT)

Front I/O:

SATA3 *6

USB 2.0 Header * 2

Serial header


USB 3.0 Header * 1

Front Audio Header

CPU FAN *1

System FAN *1

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Title INDEX			
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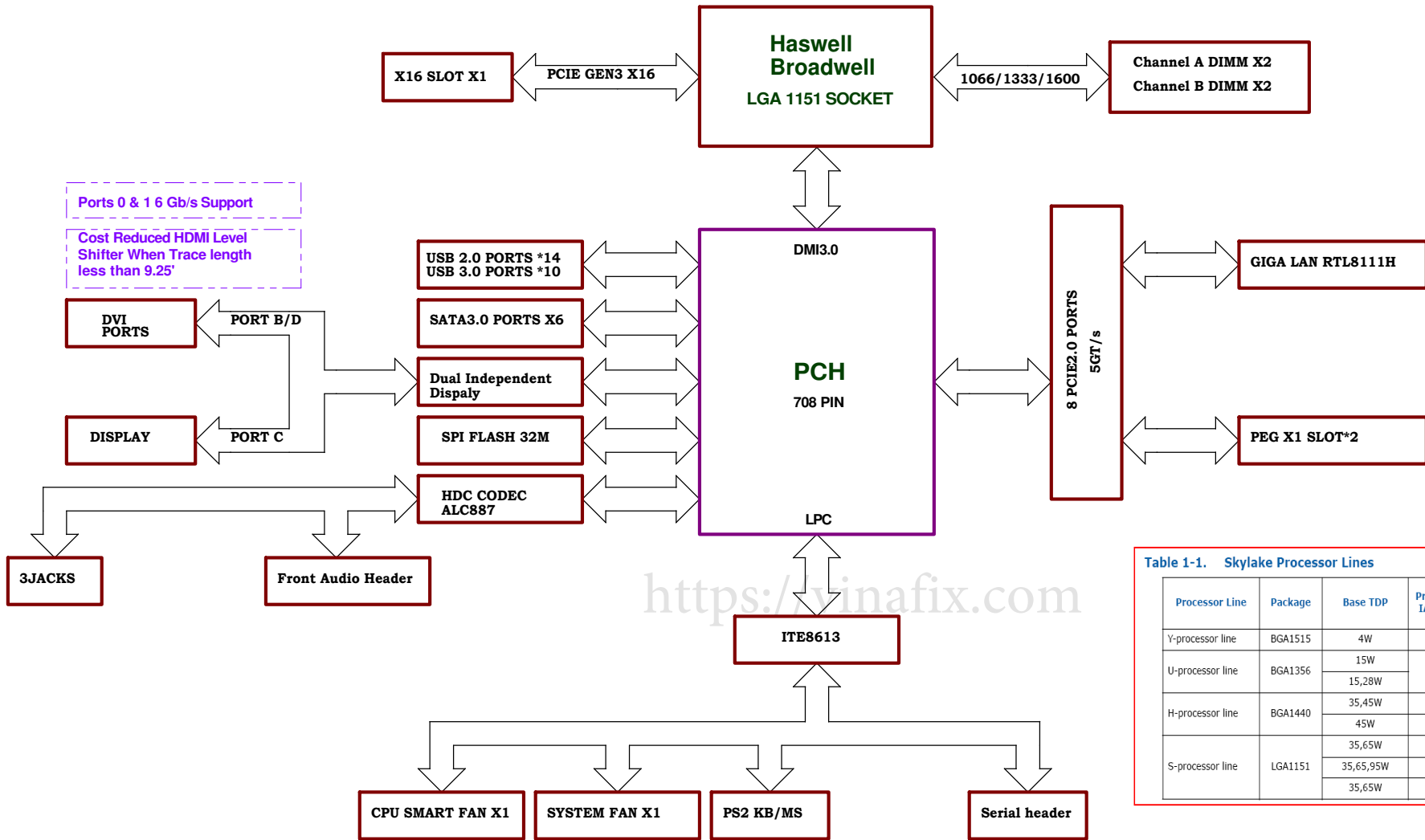



Table 1-1. Skylake Processor Lines						
Processor Line	Package	Base TDP	Processor IA Cores	Maximum Graphics Configuration	On Package Cache	Platform Type
Y-processor line	BGA1515	4W	2	GT2	N/A	1-Chip
U-processor line	BGA1356	15W	2	GT2	64 MB	1-Chip
		15,28W		GT3		
H-processor line	BGA1440	35,45W	4	GT2	N/A	2-Chip
		45W	4	GT4	128 MB	
S-processor line	LGA1151	35,65W	2	GT2	N/A	2-Chip
		35,65,95W	4	GT2		
		35,65W	4	GT4	64 MB	


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BLOCK DIAGRAM

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1.VER0.60:COLAY S3 FUNCTION(PAGE15/23/25/26/28/30/31/32/33)


2.VER0.60:COLAY REMOVE VGT_PH2(PAGE39)

3.VER0.60:DDR3 CHANGE DDR4(PAGE6/7/11/12)

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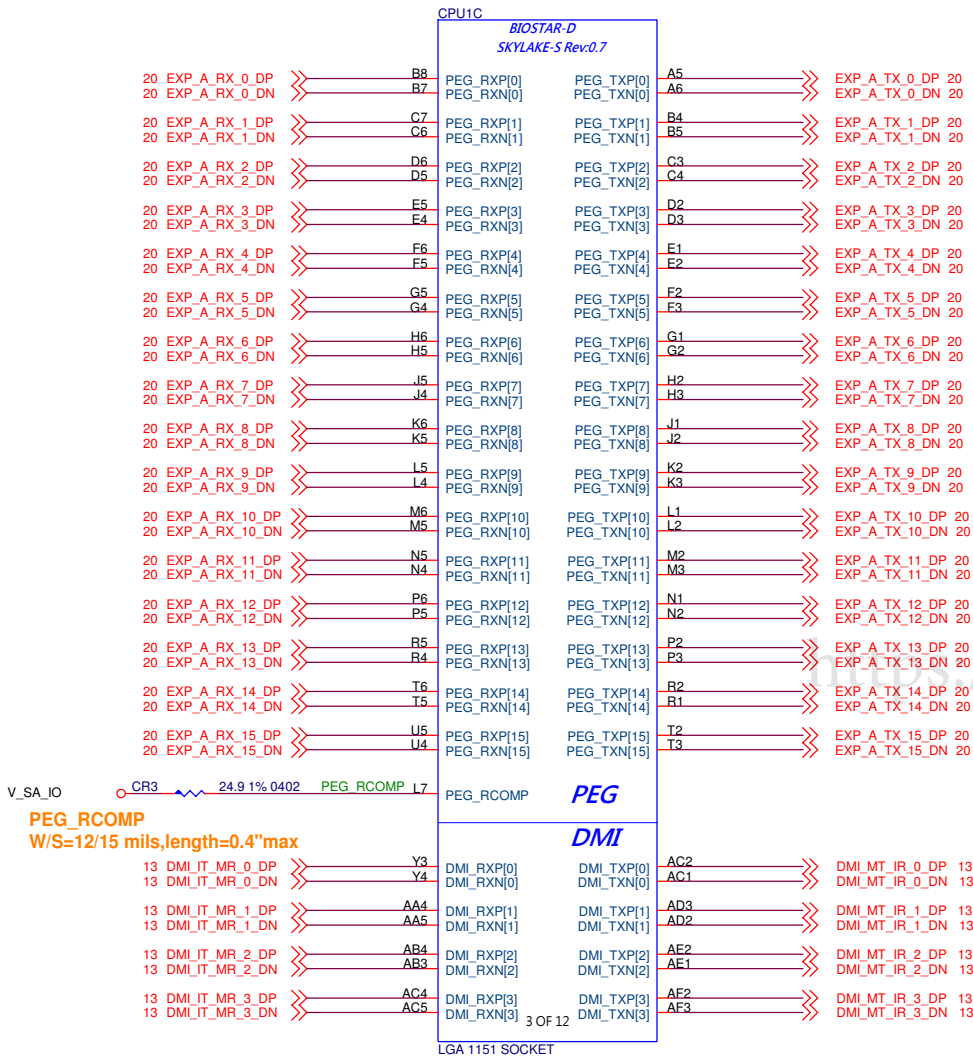
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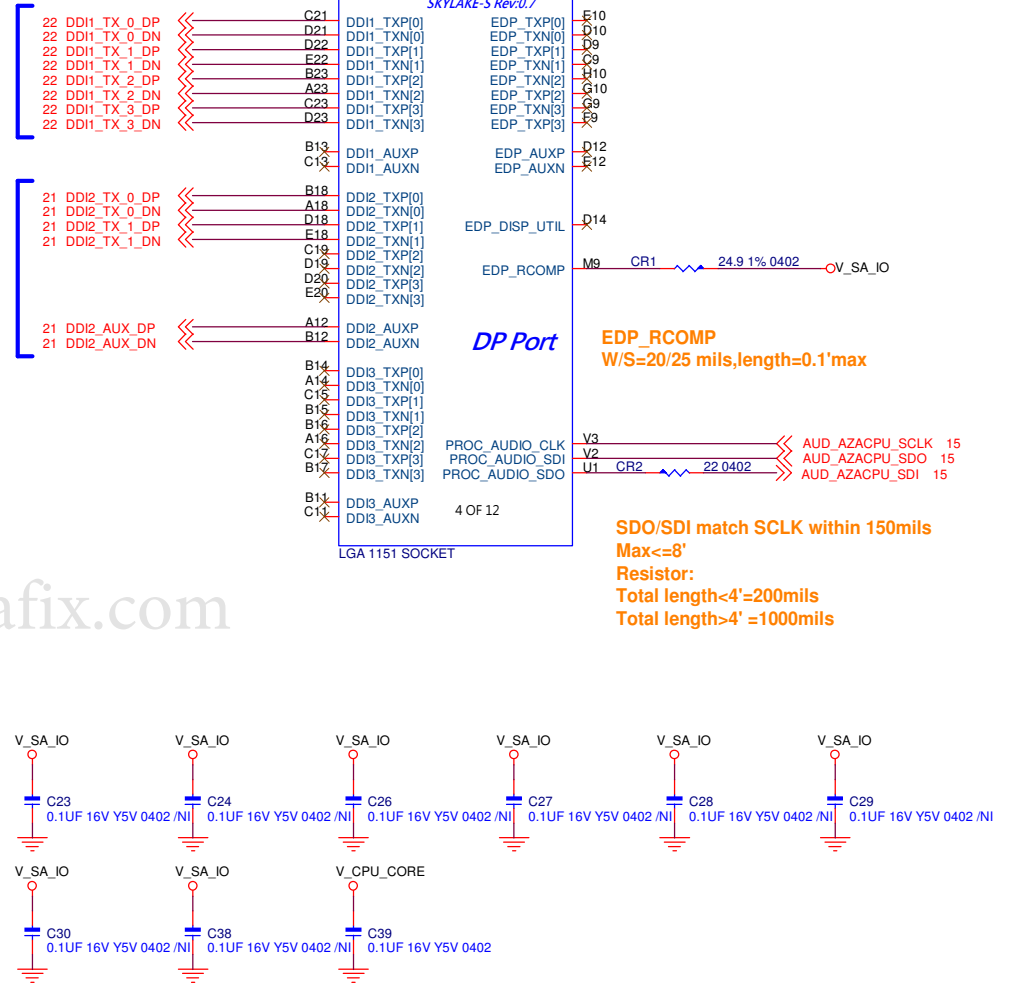
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DVI PORT

EDP to VGA



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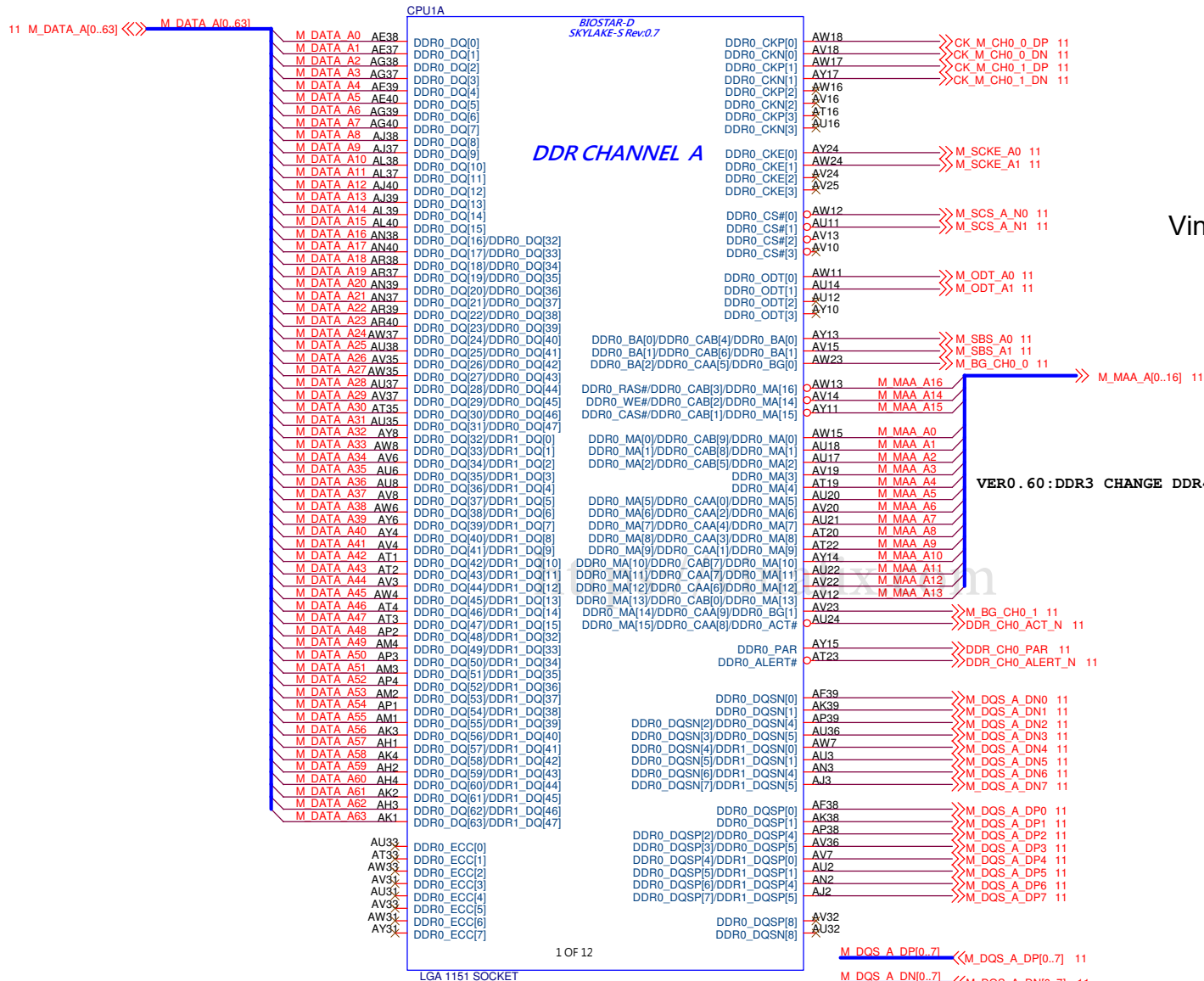
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Title
CPU PCIEX16/DMI/FDI


Size B Document Number
IH11M-MHS

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Title CPU DDR3 CHANNEL A	
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12 M_DATA_B[0..63] <<< M_DATA_B[0..63]

M_DATA_B0 AD34
M_DATA_B1 AD35
M_DATA_B2 AG35
M_DATA_B3 AH35
M_DATA_B4 AE35
M_DATA_B5 AE34
M_DATA_B6 AG34
M_DATA_B7 AH34
M_DATA_B8 AK35
M_DATA_B9 AL35
M_DATA_B10 AK32
M_DATA_B11 AL32
M_DATA_B12 AK34
M_DATA_B13 AL34
M_DATA_B14 AK31
M_DATA_B15 AL31
M_DATA_B16 AP35
M_DATA_B17 AN35
M_DATA_B18 AN32
M_DATA_B19 AP32
M_DATA_B20 AN34
M_DATA_B21 AP34
M_DATA_B22 AN31
M_DATA_B23 AP31
M_DATA_B24 AL29
M_DATA_B25 AM29
M_DATA_B26 AP29
M_DATA_B27 AR29
M_DATA_B28 AM28
M_DATA_B29 AL28
M_DATA_B30 AR28
M_DATA_B31 AP28
M_DATA_B32 AR12
M_DATA_B33 AP12
M_DATA_B34 AM13
M_DATA_B35 AL13
M_DATA_B36 AR13
M_DATA_B37 AP13
M_DATA_B38 AM12
M_DATA_B39 AL12
M_DATA_B40 AP10
M_DATA_B41 AR10
M_DATA_B42 AR7
M_DATA_B43 AP7
M_DATA_B44 AR9
M_DATA_B45 AP9
M_DATA_B46 AR6
M_DATA_B47 AP6
M_DATA_B48 AM10
M_DATA_B49 AL10
M_DATA_B50 AM7
M_DATA_B51 AL7
M_DATA_B52 AM9
M_DATA_B53 AL9
M_DATA_B54 AM6
M_DATA_B55 AL6
M_DATA_B56 AJ6
M_DATA_B57 AJ7
M_DATA_B58 AE6
M_DATA_B59 AE7
M_DATA_B60 AH7
M_DATA_B61 AH6
M_DATA_B62 AE7
M_DATA_B63 AE6

DDR1_DQ[0]/DDR0_DQ[16]
DDR1_DQ[1]/DDR0_DQ[17]
DDR1_DQ[2]/DDR0_DQ[18]
DDR1_DQ[3]/DDR0_DQ[19]
DDR1_DQ[4]/DDR0_DQ[20]
DDR1_DQ[5]/DDR0_DQ[21]
DDR1_DQ[6]/DDR0_DQ[22]
DDR1_DQ[7]/DDR0_DQ[23]
DDR1_DQ[8]/DDR0_DQ[24]
DDR1_DQ[9]/DDR0_DQ[25]
DDR1_DQ[10]/DDR0_DQ[26]
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DDR1_DQ[13]/DDR0_DQ[29]
DDR1_DQ[14]/DDR0_DQ[30]
DDR1_DQ[15]/DDR0_DQ[31]
DDR1_DQ[16]/DDR0_DQ[48]
DDR1_DQ[17]/DDR0_DQ[49]
DDR1_DQ[18]/DDR0_DQ[50]
DDR1_DQ[19]/DDR0_DQ[51]
DDR1_DQ[20]/DDR0_DQ[52]
DDR1_DQ[21]/DDR0_DQ[53]
DDR1_DQ[22]/DDR0_DQ[54]
DDR1_DQ[23]/DDR0_DQ[55]
DDR1_DQ[24]/DDR0_DQ[56]
DDR1_DQ[25]/DDR0_DQ[57]
DDR1_DQ[26]/DDR0_DQ[58]
DDR1_DQ[27]/DDR0_DQ[59]
DDR1_DQ[28]/DDR0_DQ[60]
DDR1_DQ[29]/DDR0_DQ[61]
DDR1_DQ[30]/DDR0_DQ[62]
DDR1_DQ[31]/DDR0_DQ[63]
DDR1_DQ[32]/DDR1_DQ[16]
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DDR1_DQ[46]/DDR1_DQ[30]
DDR1_DQ[47]/DDR1_DQ[31]
DDR1_DQ[48]
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DDR1_DQ[50]
DDR1_DQ[51]
DDR1_DQ[52]
DDR1_DQ[53]
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DDR1_DQ[58]
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DDR1_DQ[60]
DDR1_DQ[61]
DDR1_DQ[62]
DDR1_DQ[63]
DDR1_ECC[0]
DDR1_ECC[1]
DDR1_ECC[2]
DDR1_ECC[3]
DDR1_ECC[4]
DDR1_ECC[5]
DDR1_ECC[6]
DDR1_ECC[7]

AR25
AR26
AM26
AM25
AP26
AP25
AL25
AL26

LGA 1151 SOCKET

BIOSTAR-D
SKYLAKE-S
Rev:0.7

DDR CHANNEL B

DDR1_RAS#/DDR1_CAB[3]/DDR1_MA[16]
DDR1_WE#/DDR1_CAB[2]/DDR1_MA[14]
DDR1_CAS#/DDR1_CAB[1]/DDR1_MA[15]

DDR1_BA[0]/DDR1_CAB[4]/DDR1_BA[0]
DDR1_BA[1]/DDR1_CAB[6]/DDR1_BA[1]
DDR1_BA[2]/DDR1_CAB[5]/DDR1_BG[0]

DDR1_MA[0]/DDR1_CAB[9]/DDR1_MA[0]
DDR1_MA[1]/DDR1_CAB[8]/DDR1_MA[1]
DDR1_MA[2]/DDR1_CAB[5]/DDR1_MA[2]

DDR1_MA[5]/DDR1_CAA[0]/DDR1_MA[5]
DDR1_MA[6]/DDR1_CAA[2]/DDR1_MA[6]
DDR1_MA[7]/DDR1_CAA[4]/DDR1_MA[7]
DDR1_MA[8]/DDR1_CAA[3]/DDR1_MA[8]
DDR1_MA[9]/DDR1_CAA[1]/DDR1_MA[9]
DDR1_MA[10]/DDR1_CAB[7]/DDR1_MA[10]
DDR1_MA[11]/DDR1_CAA[7]/DDR1_MA[11]
DDR1_MA[12]/DDR1_CAA[6]/DDR1_MA[12]
DDR1_MA[13]/DDR1_CAB[0]/DDR1_MA[13]
DDR1_MA[14]/DDR1_CAA[9]/DDR1_BG[1]
DDR1_MA[15]/DDR1_CAA[8]/DDR1_ACT#

DDR1_PAR
DDR1_ALERT#

DDR1_DQSN[0]/DDR0_DQSN[2]
DDR1_DQSN[1]/DDR0_DQSN[3]
DDR1_DQSN[2]/DDR0_DQSN[6]
DDR1_DQSN[3]/DDR0_DQSN[7]
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DDR1_DQSP[7]

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DDR1_DQSN[8]

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DDR1_VREF_DQ

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DDR1_CKN[3]

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DDR1_MAA_B7
DDR1_MAA_B8
DDR1_MAA_B9
DDR1_MAA_B10
DDR1_MAA_B11
DDR1_MAA_B12
DDR1_MAA_B13

AM20 >>> CK_M_CH1_0_DP 12
AM21 >>> CK_M_CH1_0_DN 12
AP22 >>> CK_M_CH1_1_DP 12
AP21 >>> CK_M_CH1_1_DN 12
AN20
AN21
AP19
AP20

AY29 >>> M_SCKE_B0 12
AV29 >>> M_SCKE_B1 12
AW29
AU29

AP17 >>> M_SCS_B_N0 12
AN15 >>> M_SCS_B_N1 12
AN17
AM15

AM16 >>> M_ODT_B0 12
AL16 >>> M_ODT_B1 12
AP15
AL15

AN18 M MAA_B16 >>> M_MAA_B[0..16] 12
AL17 M MAA_B14 >>> M_MAA_B[0..16] 12
AP16 M MAA_B15 >>> M_MAA_B[0..16] 12

AL18 >>> M_SBS_B0 12
AM18 >>> M_SBS_B1 12
AW28 >>> M_BG_CH1_0 12

AL19 M MAA_B0 >>> M_MAA_B[0..16] 12
AL22 M MAA_B1 >>> M_MAA_B[0..16] 12
AM22 M MAA_B2 >>> M_MAA_B[0..16] 12
AM23 M MAA_B3 >>> M_MAA_B[0..16] 12
AP23 M MAA_B4 >>> M_MAA_B[0..16] 12
AM24 M MAA_B5 >>> M_MAA_B[0..16] 12
AW24 M MAA_B6 >>> M_MAA_B[0..16] 12
AY26 M MAA_B7 >>> M_MAA_B[0..16] 12
AU26 M MAA_B8 >>> M_MAA_B[0..16] 12
AW27 M MAA_B9 >>> M_MAA_B[0..16] 12
AP18 M MAA_B10 >>> M_MAA_B[0..16] 12
AU27 M MAA_B11 >>> M_MAA_B[0..16] 12
AV27 M MAA_B12 >>> M_MAA_B[0..16] 12
AR15 M MAA_B13 >>> M_MAA_B[0..16] 12

AY28 >>> M_BG_CH1_1 12
AU28 >>> DDR_CH1_ACT_N 12

AL20 >>> DDR_CH1_PAR 12
AY25 >>> DDR_CH1_ALERT_N 12

AF34 >>> M_DQS_B_DN0 12
AK33 >>> M_DQS_B_DN1 12
AN33 >>> M_DQS_B_DN2 12
AN29 >>> M_DQS_B_DN3 12
AN13 >>> M_DQS_B_DN4 12
AR8 >>> M_DQS_B_DN5 12
AM8 >>> M_DQS_B_DN6 12
AG6 >>> M_DQS_B_DN7 12

AF35 >>> M_DQS_B_DP0 12
AL33 >>> M_DQS_B_DP1 12
AP33 >>> M_DQS_B_DP2 12
AN28 >>> M_DQS_B_DP3 12
AN12 >>> M_DQS_B_DP4 12
AP8 >>> M_DQS_B_DP5 12
AL8 >>> M_DQS_B_DP6 12
AG7 >>> M_DQS_B_DP7 12

AN25 >>> M_DQS_B_DP8 12
AN26 >>> M_DQS_B_DP9 12

AB40 CPU VREF_DIMMA >>> CPU_VREF_DIMMA 11
AC40 DDR0_VREF_DQ >>> CPU_VREF_DIMMA 11
AC39 CPU VREF_DIMMB >>> CPU_VREF_DIMMB 12

M_DQS_B_DP0_7 >>> M_DQS_B_DP[0..7] 12
M_DQS_B_DN0_7 >>> M_DQS_B_DN[0..7] 12

M_DQS_B_DP0_7 >>> M_DQS_B_DP[0..7] 12
M_DQS_B_DN0_7 >>> M_DQS_B_DN[0..7] 12

M_DQS_B_DP0_7 >>> M_DQS_B_DP[0..7] 12
M_DQS_B_DN0_7 >>> M_DQS_B_DN[0..7] 12

M_DQS_B_DP0_7 >>> M_DQS_B_DP[0..7] 12
M_DQS_B_DN0_7 >>> M_DQS_B_DN[0..7] 12

M_DQS_B_DP0_7 >>> M_DQS_B_DP[0..7] 12
M_DQS_B_DN0_7 >>> M_DQS_B_DN[0..7] 12

M_DQS_B_DP0_7 >>> M_DQS_B_DP[0..7] 12
M_DQS_B_DN0_7 >>> M_DQS_B_DN[0..7] 12

M_DQS_B_DP0_7 >>> M_DQS_B_DP[0..7] 12
M_DQS_B_DN0_7 >>> M_DQS_B_DN[0..7] 12

M_DQS_B_DP0_7 >>> M_DQS_B_DP[0..7] 12
M_DQS_B_DN0_7 >>> M_DQS_B_DN[0..7] 12

M_DQS_B_DP0_7 >>> M_DQS_B_DP[0..7] 12
M_DQS_B_DN0_7 >>> M_DQS_B_DN[0..7] 12

M_DQS_B_DP0_7 >>> M_DQS_B_DP[0..7] 12
M_DQS_B_DN0_7 >>> M_DQS_B_DN[0..7] 12

M_DQS_B_DP0_7 >>> M_DQS_B_DP[0..7] 12
M_DQS_B_DN0_7 >>> M_DQS_B_DN[0..7] 12

M_DQS_B_DP0_7 >>> M_DQS_B_DP[0..7] 12
M_DQS_B_DN0_7 >>> M_DQS_B_DN[0..7] 12

M_DQS_B_DP0_7 >>> M_DQS_B_DP[0..7] 12
M_DQS_B_DN0_7 >>> M_DQS_B_DN[0..7] 12

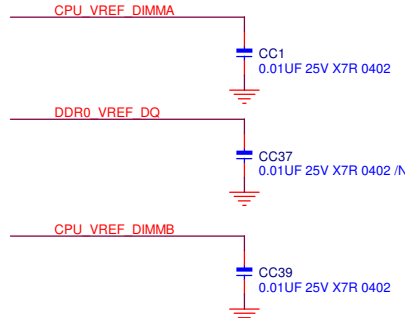
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M_DQS_B_DN0_7 >>> M_DQS_B_DN[0..7] 12

M_DQS_B_DP0_7 >>> M_DQS_B_DP[0..7] 12
M_DQS_B_DN0_7 >>> M_DQS_B_DN[0..7] 12

M_DQS_B_DP0_7 >>> M_DQS_B_DP[0..7] 12
M_DQS_B_DN0_7 >>> M_DQS_B_DN[0..7] 12

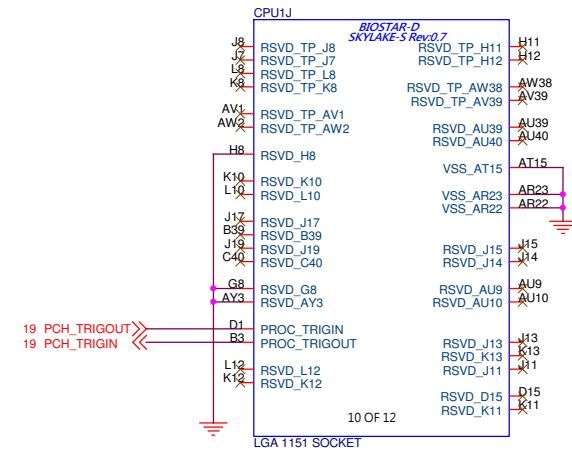
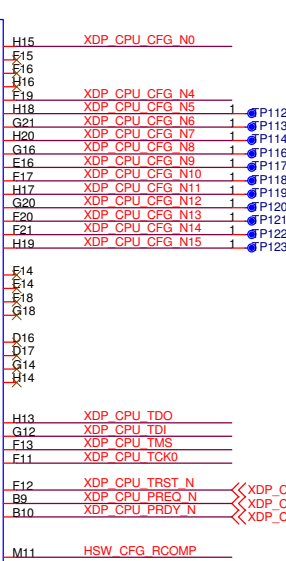
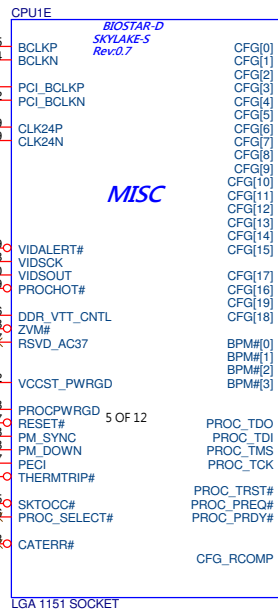
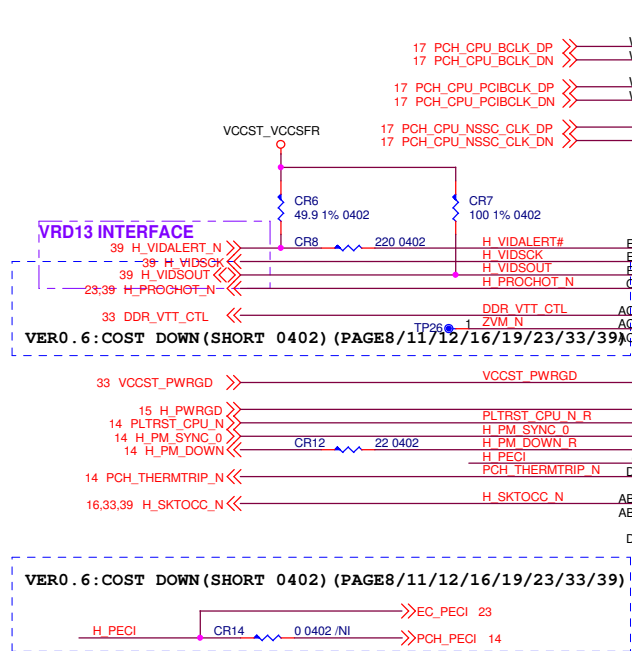
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M_DQS_B_DN0_7 >>> M_DQS_B_DN[0..7] 12

M_DQS_B_DP0_7 >>> M_DQS_B_DP[0..7] 12
M_DQS_B_DN0_7 >>> M_DQS_B_DN[0..7] 12



Title CPU DDR3 CHANNEL B

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CFG	HIGH	LOW	STRAP DESCRIPTION
0	NORMAL	STALL	EAR
1	NORMAL	PCHLESS	PCHLESS MODE
2	NORMAL	REVERSE	PEG_LANE_REVERSAL
3	ENABLE	DISABLE	PHYSICAL_DEBUG_ENABLE
4	DISABLE	ENABLE	DP PRESENCE
5	DISABLE	ENABLE	PEG0CFGSEL[0]
6	DISABLE	ENABLE	PEG0CFGSEL[1]
7	RESET_N	BIOS REQ	PEG_DEFER_TRAINING
8	DISABLE	ENABLE	CFG_UNLOCK
9	PRESENT	NOT PRESENT	SVID NOT PRESENT
10	ACTIVATE	DEACTIVATE	SAFE MODE BOOT
11	DC COUPLED	AC COUPLED	DMI_AC_COUPLED
12	PMSYNC 2.0	LEGACY	PMSYNC LEGACY
13	SYNC	ASYN	PMSYNC ASYN MODE
14	RESERVED		
15	RESERVED		

ALL PINS HAVE INTERNAL PULL-UPS

Bifurcation	Link Width			Config. Signals		
	0:1:0	0:1:1	0:1:2	CFG [6]	CFG [5]	CFG [2]
1x16	x16	N/A	N/A	1	1	1
1x16 Reversed	x16	N/A	N/A	1	1	0
2x8	x8	x8	N/A	1	0	1
2x8 Reversed	x8	x8	N/A	1	0	0
1x8+2x4	x8	x4	x4	0	0	1
1x8+2x4 Reversed	x8	x4	x4	0	0	0

CFG[19:0]	<p>Configuration Signals: The CFG signals have a default value of 1. If not terminated on the board, refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired.</p> <ul style="list-style-type: none"> CFG[0]: Stall reset sequence after PCI PUL lock until de-asserted. <ul style="list-style-type: none"> 1 = (Default) Normal Operation; No stall. CFG[1]: Reserved configuration lane. CFG[2]: PCI Express* Static x10 Lane Numbering Reversal. <ul style="list-style-type: none"> 1 = Normal operation 0 = Lane numbers reversed. CFG[3]: Reserved configuration lane. CFG[4]: eDP enable. <ul style="list-style-type: none"> 1 = Enabled. 0 = Disabled. CFG[5]: PCI Express* Bifurcation. <ul style="list-style-type: none"> 00 = 1 x8, 2 x4 PCI Express* 01 = reserved 10 = 2 x8 PCI Express* 11 = 1 x16 PCI Express* CFG[7]: PEG Training. <ul style="list-style-type: none"> 0 = (Default) PEG Training immediately following RESET# de-assertion. 1 = PEG Wait for BIOS for training. CFG[10:15]: Reserved configuration lanes.
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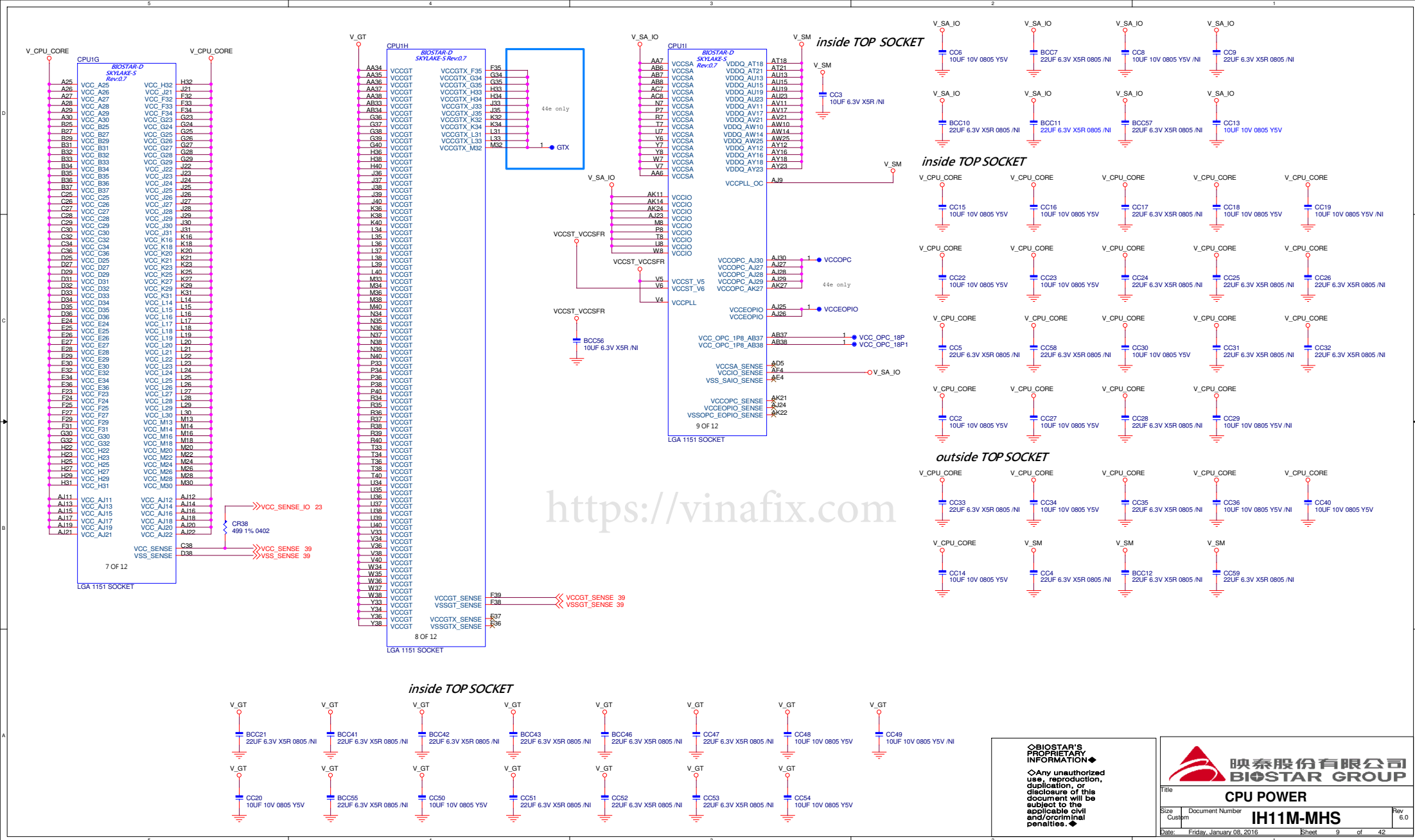
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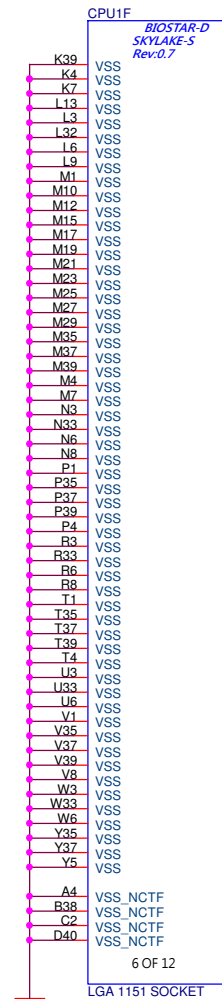
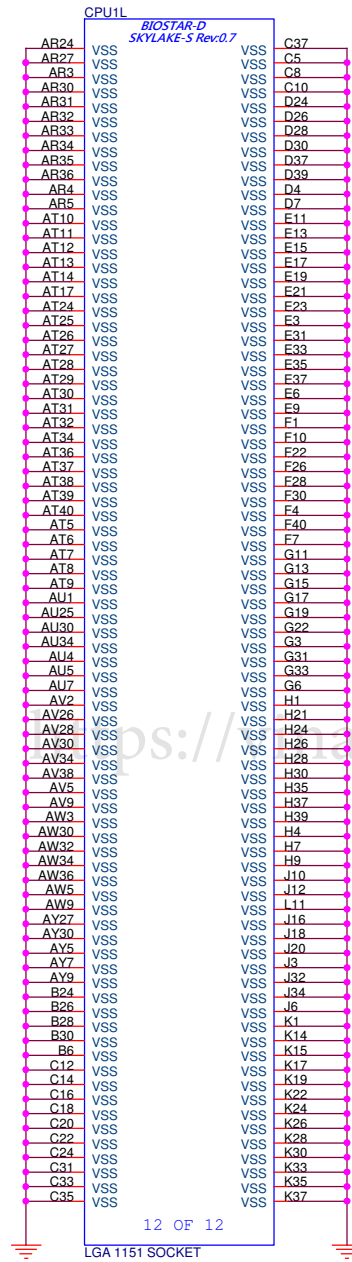
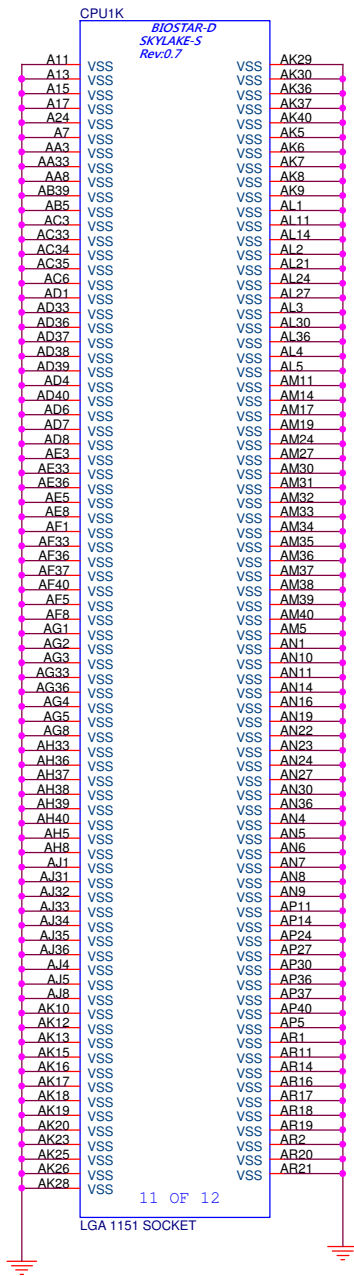
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CPU MISC

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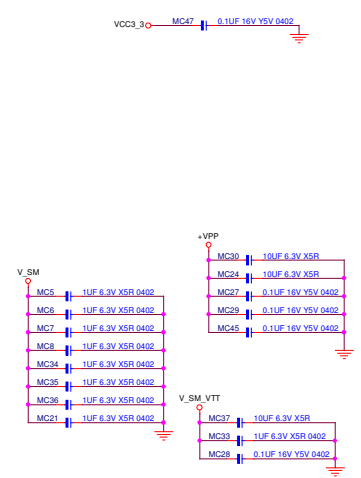
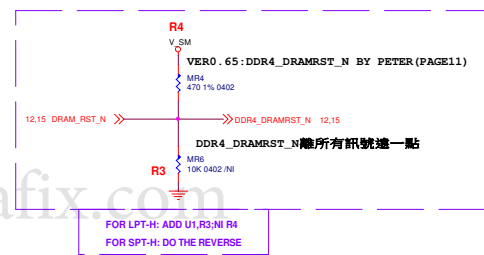
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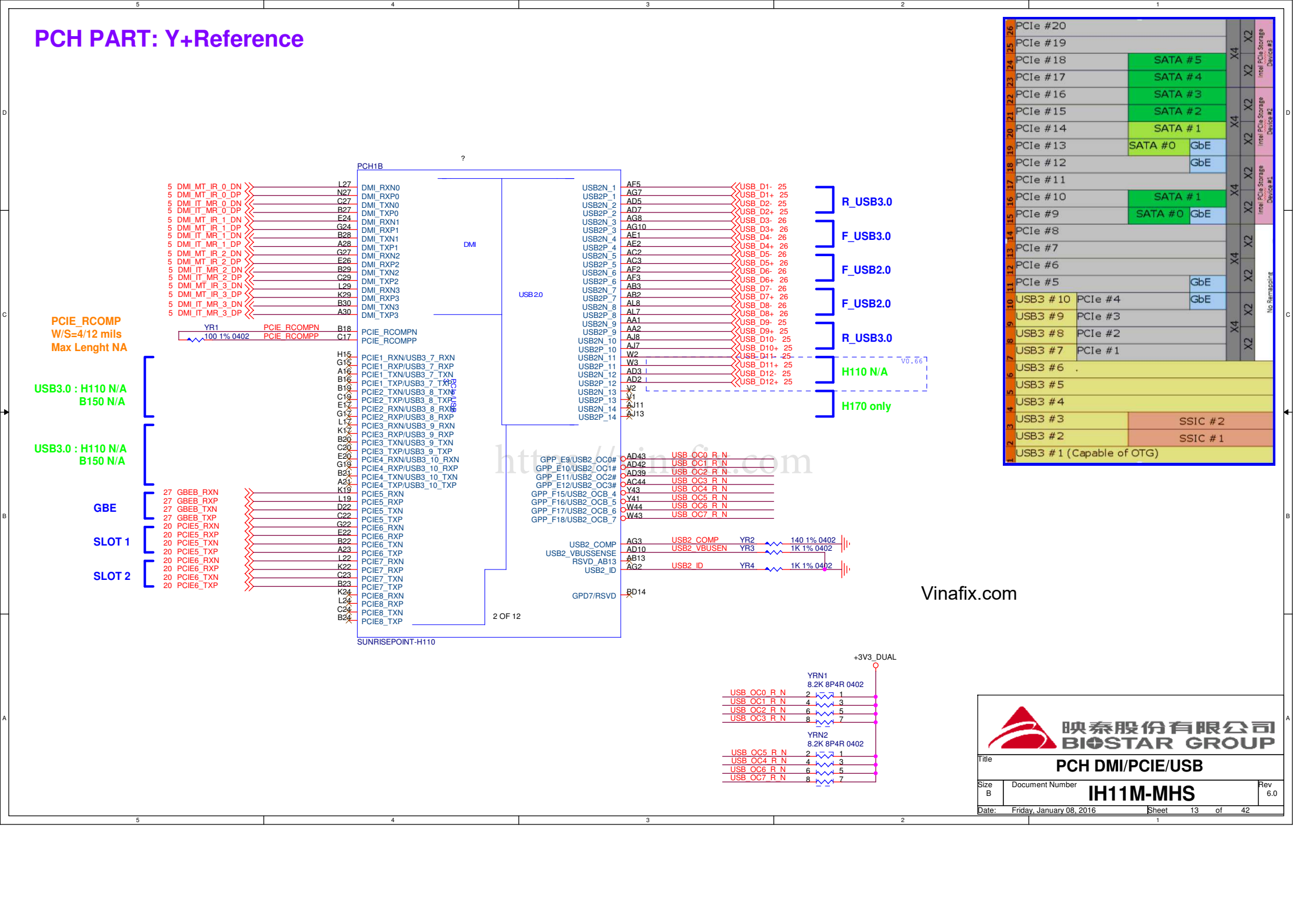
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Title		
CPU GND		
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[illegible]

PCH PART: Y+Reference

PCIE_RCOMP
W/S=4/12 mils
Max Lenght NA

USB3.0 : H110 N/A
B150 N/A

USB3.0 : H110 N/A
B150 N/A

GBE

SLOT 1

SLOT 2

PCIE #20

PCIE #19

PCIE #18

PCIE #17

PCIE #16

PCIE #15

PCIE #14

PCIE #13

PCIE #12

PCIE #11

PCIE #10

PCIE #9

PCIE #8

PCIE #7

PCIE #6

PCIE #5

PCIE #4

PCIE #3

PCIE #2

PCIE #1

USB3 #10

USB3 #9

USB3 #8

USB3 #7

USB3 #6

USB3 #5

USB3 #4

USB3 #3

USB3 #2

USB3 #1 (Capable of OTG)

SSIC #2

SSIC #1

Intel PCH Storage Device #3

Intel PCH Storage Device #2

Intel PCH Storage Device #1

No Remapping

YR1
100 1% 0402

PCIE_RCOMP
PCIE_RCOMP
PCIE_RCOMP

PCIE1_RXN/USB3_7_RXN

PCIE1_RXP/USB3_7_RXP

PCIE1_TXN/USB3_7_TXN

PCIE1_TXP/USB3_7_TXP

PCIE2_RXN/USB3_8_RXN

PCIE2_RXP/USB3_8_RXP

PCIE2_TXN/USB3_8_TXN

PCIE2_TXP/USB3_8_TXP

PCIE3_RXN/USB3_9_RXN

PCIE3_RXP/USB3_9_RXP

PCIE3_TXN/USB3_9_TXN

PCIE3_TXP/USB3_9_TXP

PCIE4_RXN/USB3_10_RXN

PCIE4_RXP/USB3_10_RXP

PCIE4_TXN/USB3_10_TXN

PCIE4_TXP/USB3_10_TXP

PCIE5_RXN

PCIE5_RXP

PCIE5_TXN

PCIE5_TXP

PCIE6_RXN

PCIE6_RXP

PCIE6_TXN

PCIE6_TXP

PCIE7_RXN

PCIE7_RXP

PCIE7_TXN

PCIE7_TXP

PCIE8_RXN

PCIE8_RXP

PCIE8_TXN

PCIE8_TXP

GPP_E9/USB2_OC0#

GPP_E10/USB2_OC1#

GPP_E11/USB2_OC2#

GPP_E12/USB2_OC3#

GPP_F15/USB2_OCB_4

GPP_F16/USB2_OCB_5

GPP_F17/USB2_OCB_6

GPP_F18/USB2_OCB_7

USB2_COMP

USB2_VBUSSENSE

RSVD_AB13

USB2_ID

GPD7/RSVD

YR2
140 1% 0402

YR3
1K 1% 0402

YR4
1K 1% 0402

YRN1
8.2K 8P4R 0402

YRN2
8.2K 8P4R 0402

USB_OC0_R_N

USB_OC1_R_N

USB_OC2_R_N

USB_OC3_R_N

USB_OC5_R_N

USB_OC4_R_N

USB_OC6_R_N

USB_OC7_R_N

+3V3_DUAL

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BIOSTAR GROUP

Title
PCH DMI/PCIE/USB

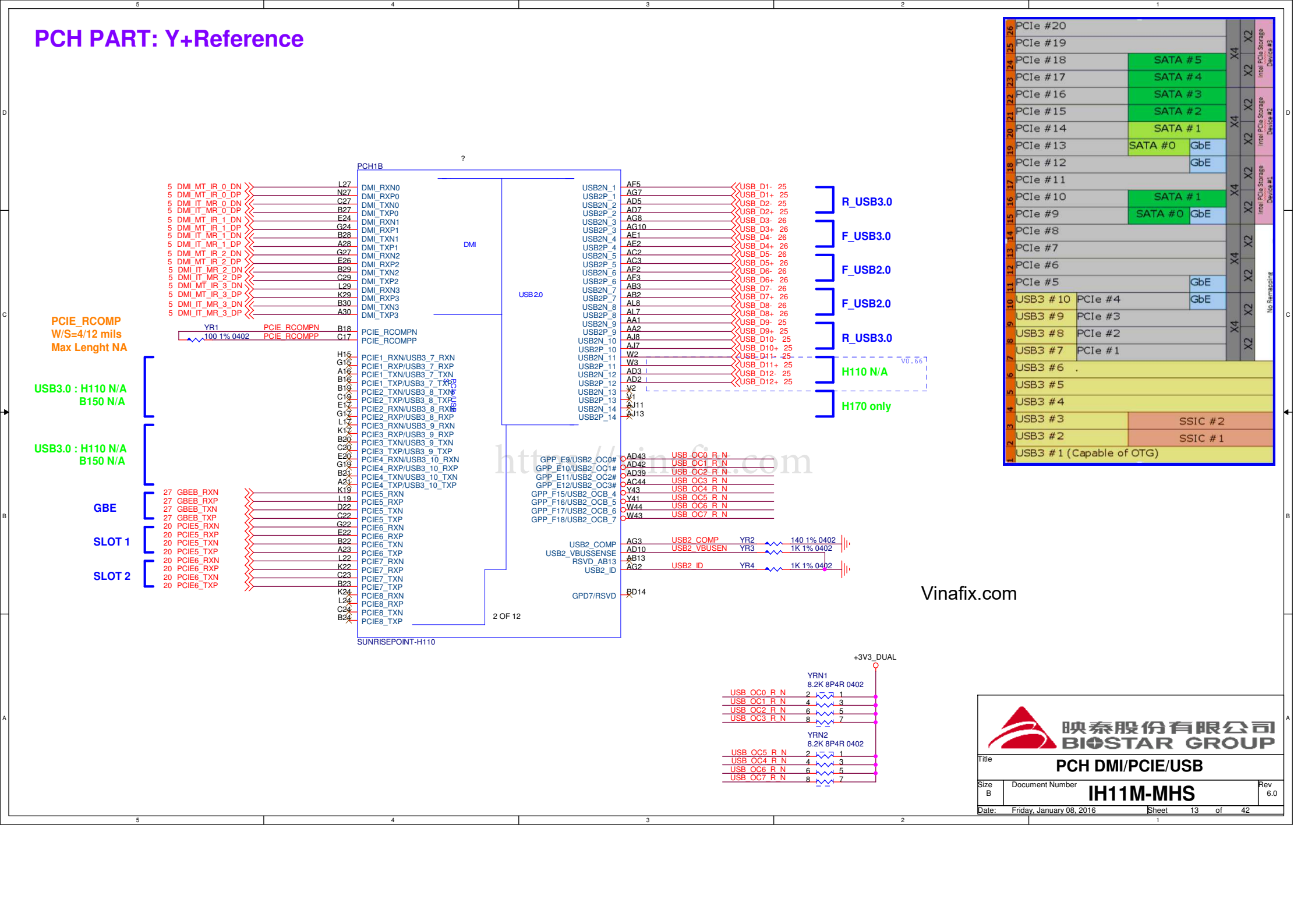
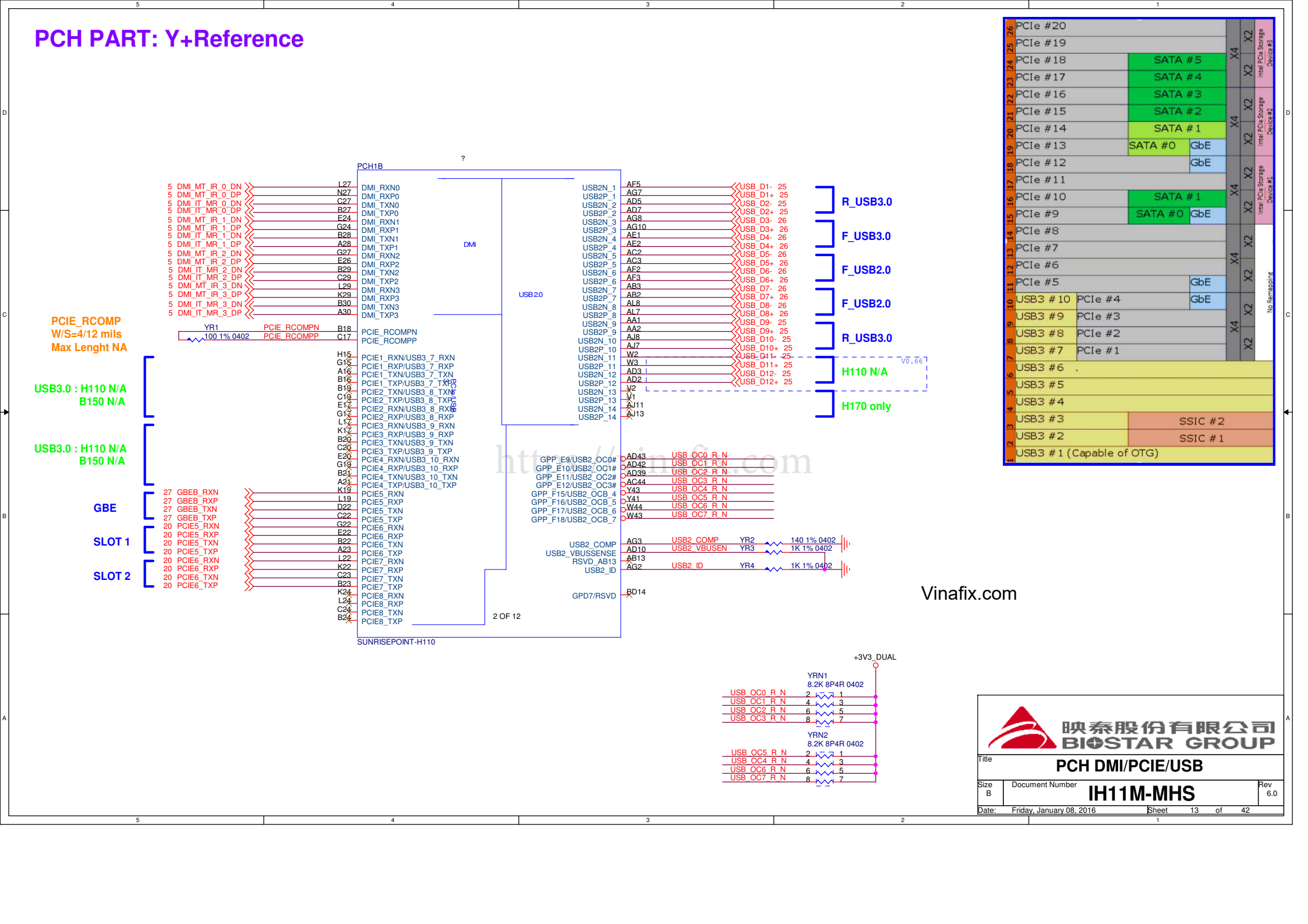
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Document Number
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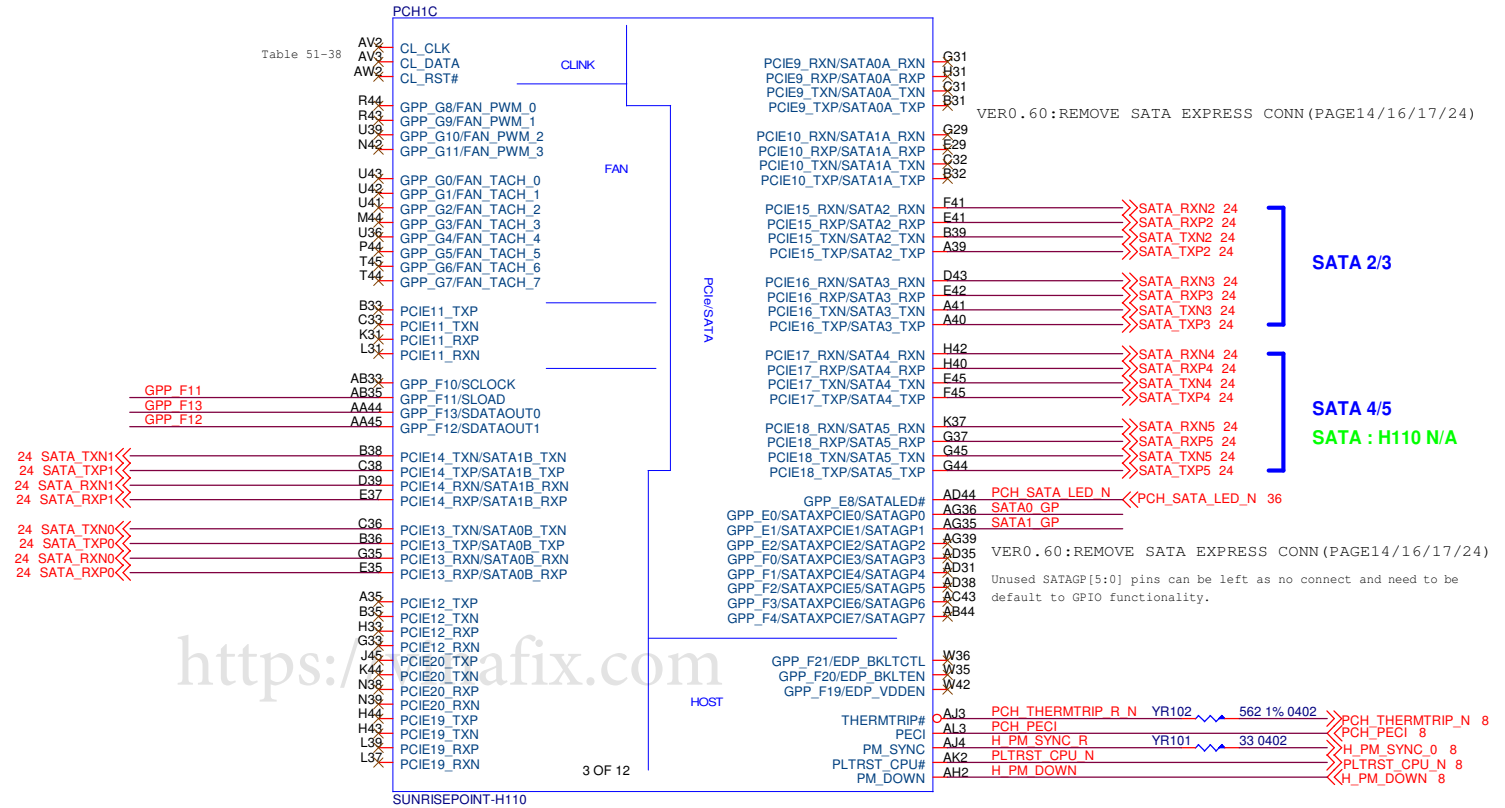
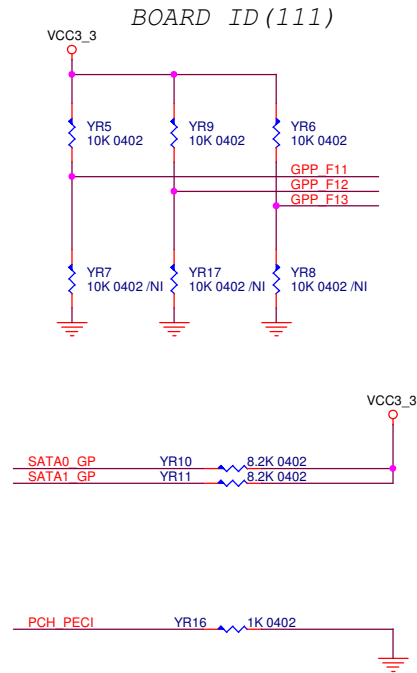
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PCH PART: Y+Reference



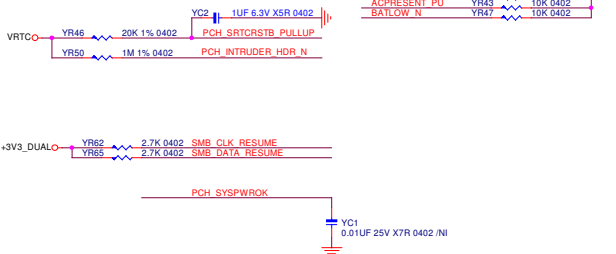
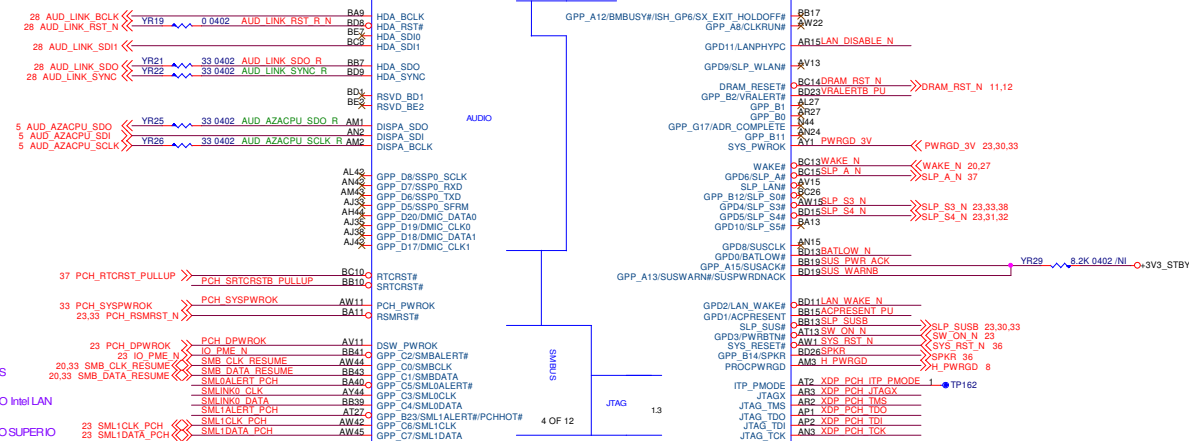
GbE can be mapped into one of the PCIe Ports 4-5, Port 9, and Ports 12-13.

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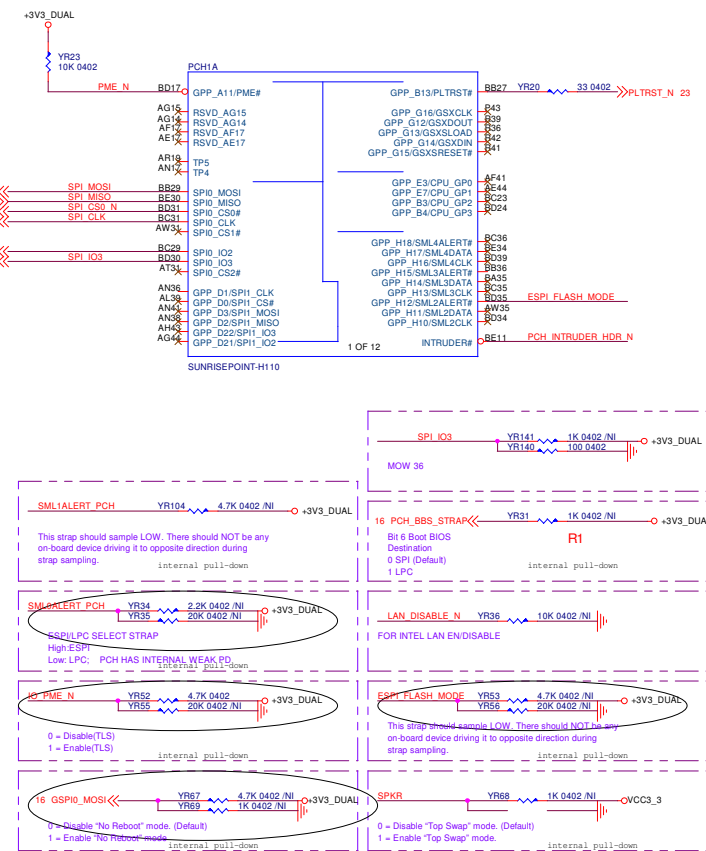
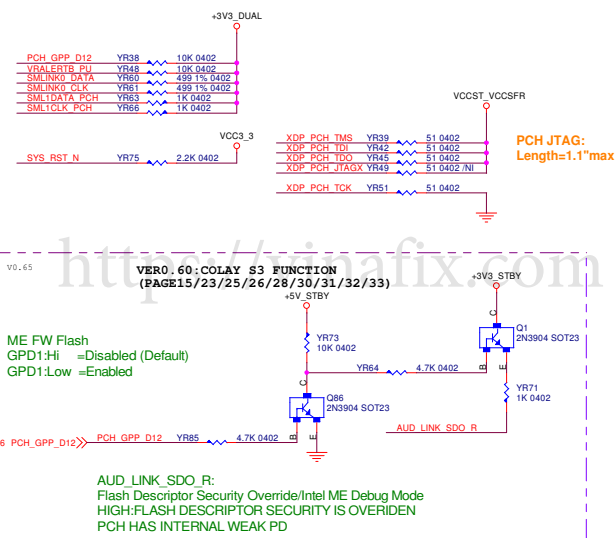
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PCH CLINK/SATA/CPU HOST			
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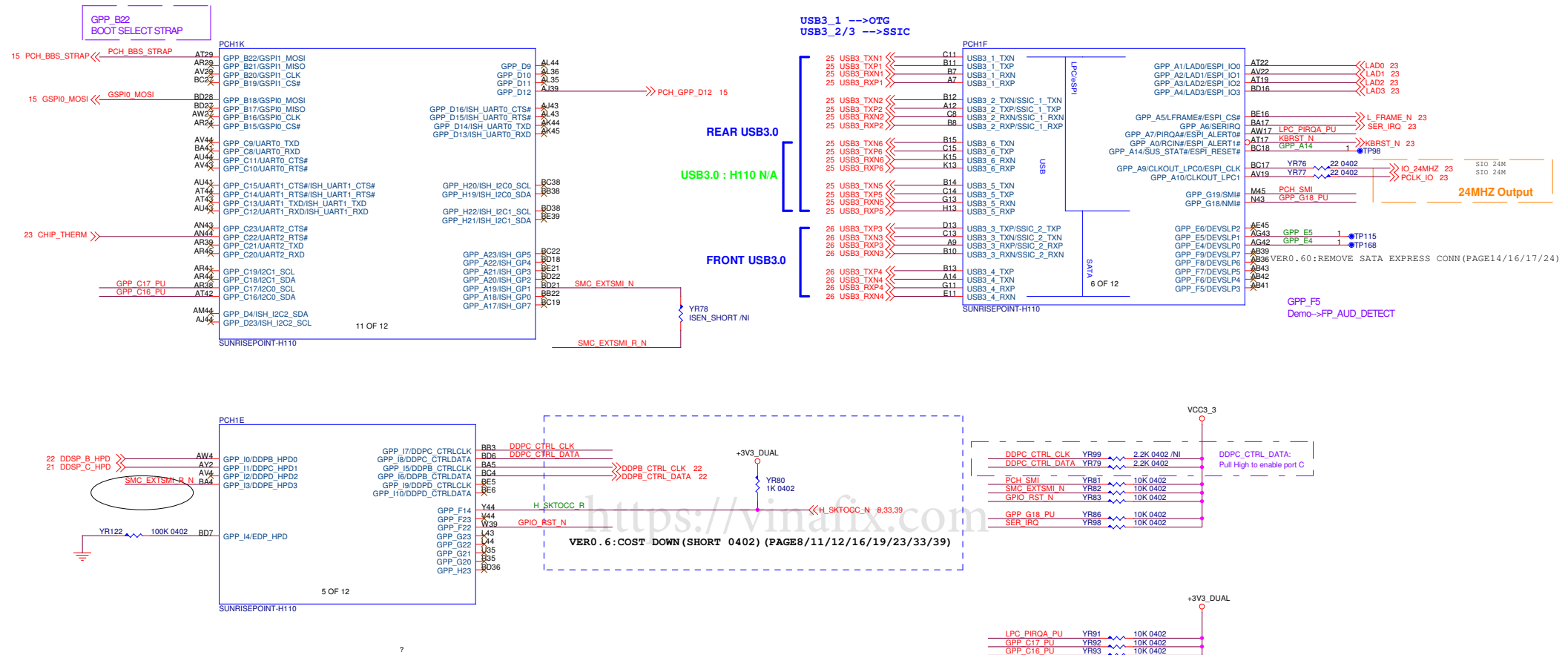


Title	PCH LPC/HDA/SPI/MISC
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Custom		

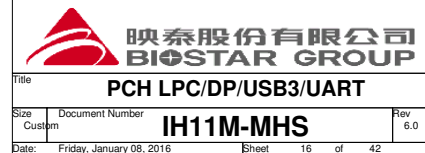
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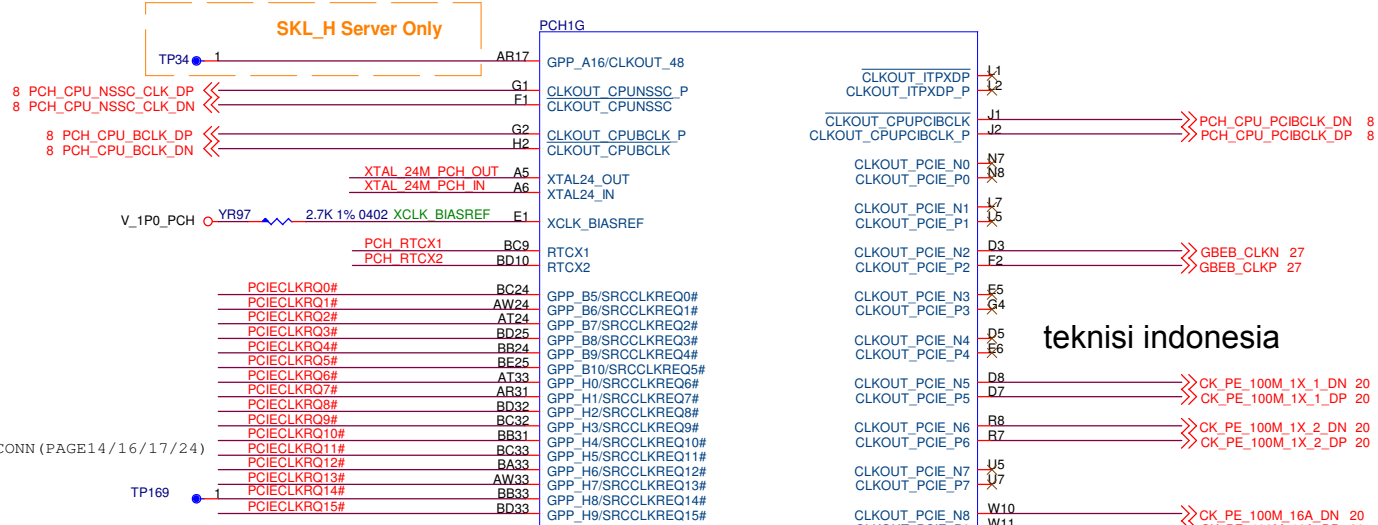
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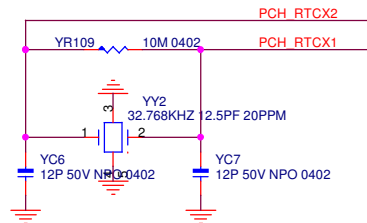
RTL 8111H


PCIE X1

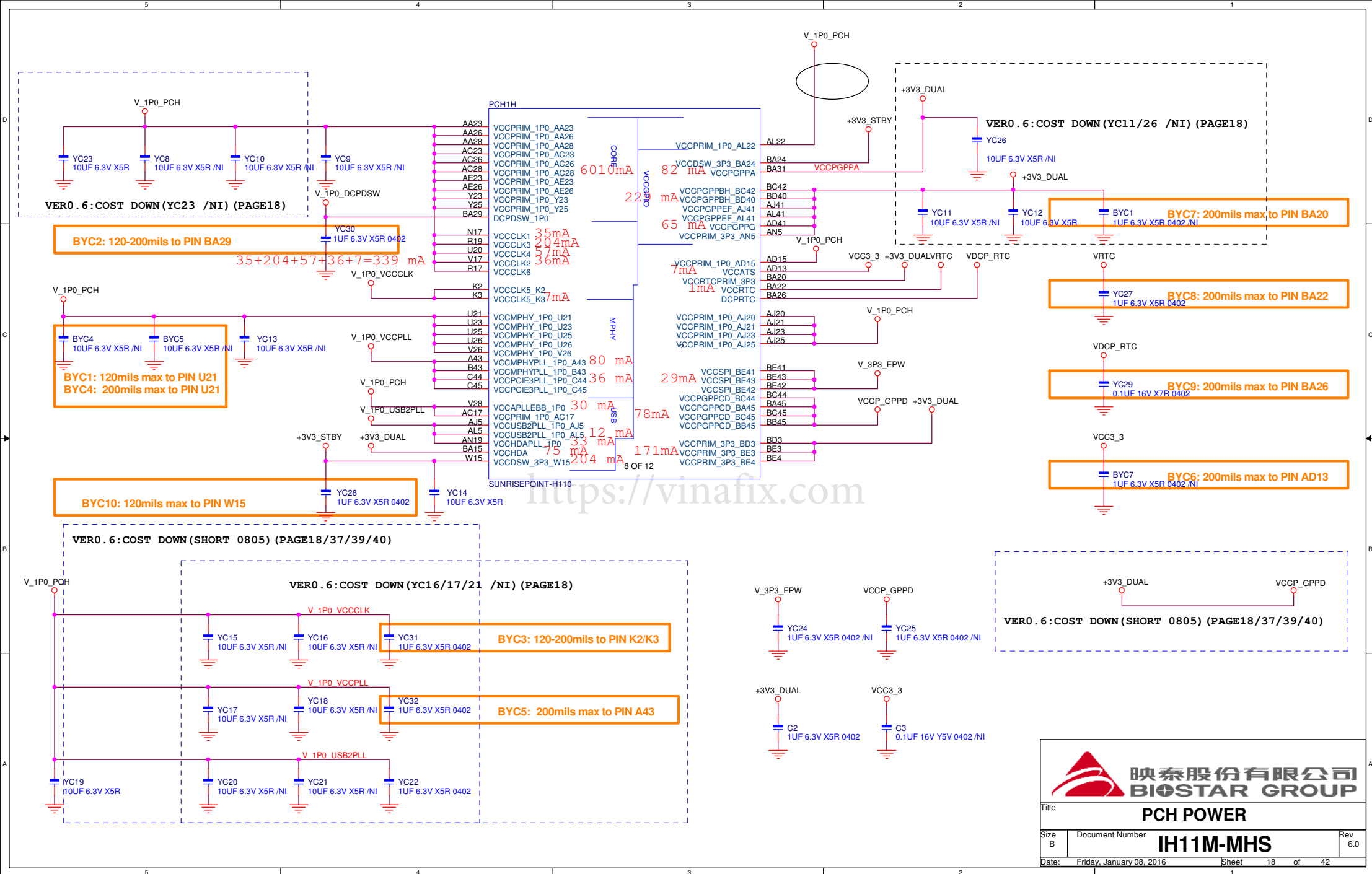
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PCIE X16

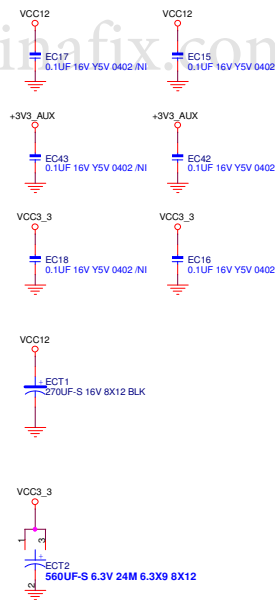
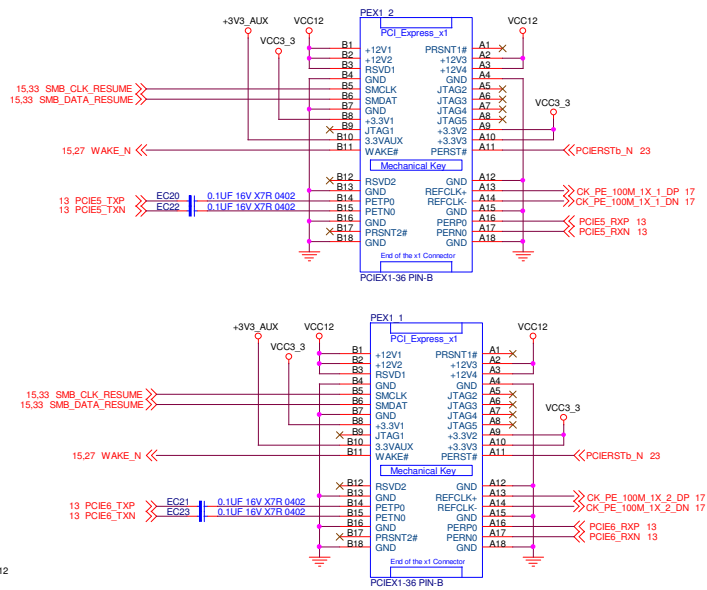
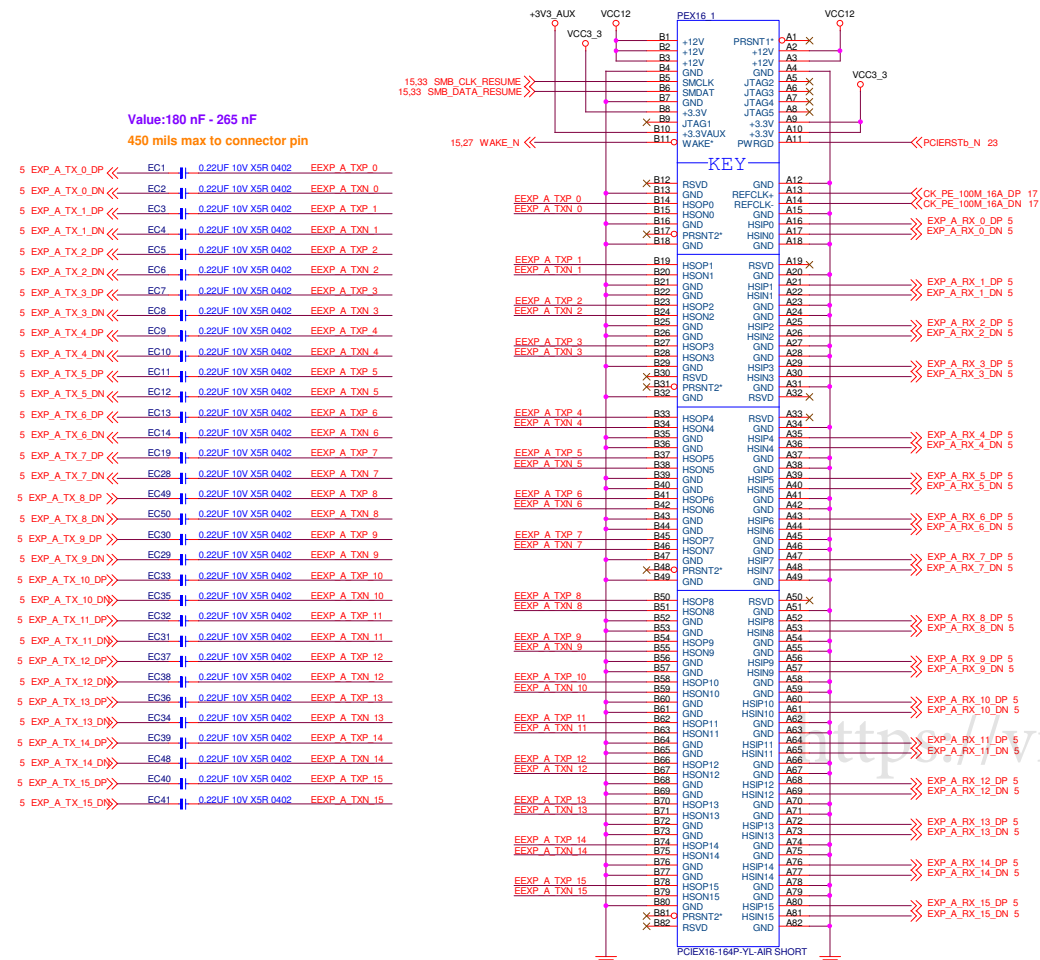
RTC CRYSTAL



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Title PCH CLOCK BUFFER			
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SLOT PART: E+Reference



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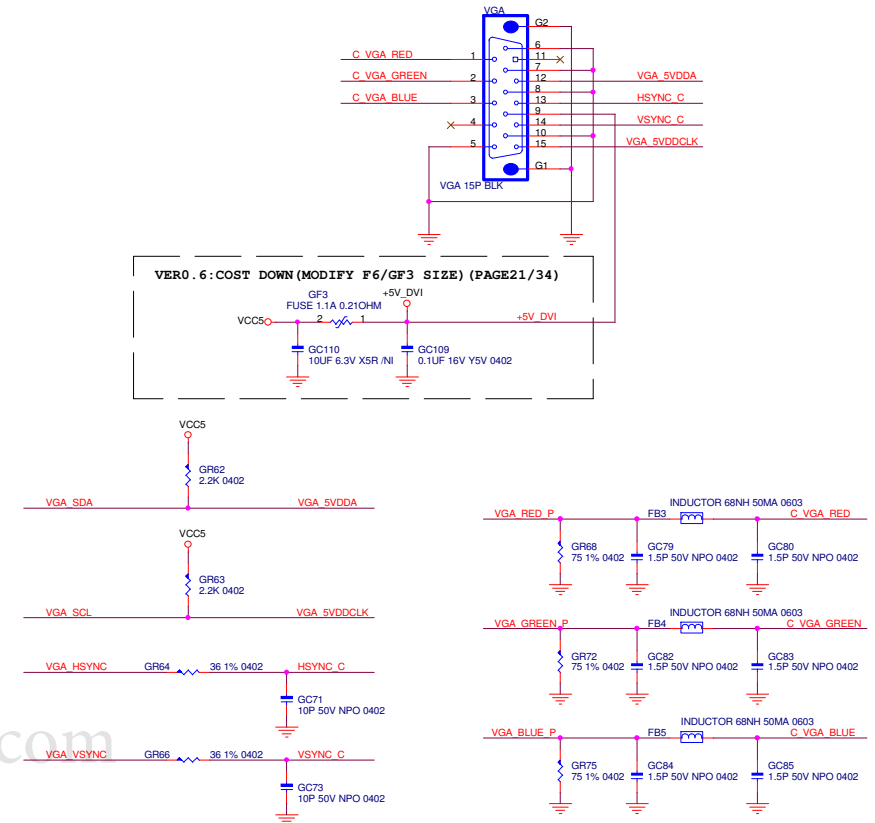
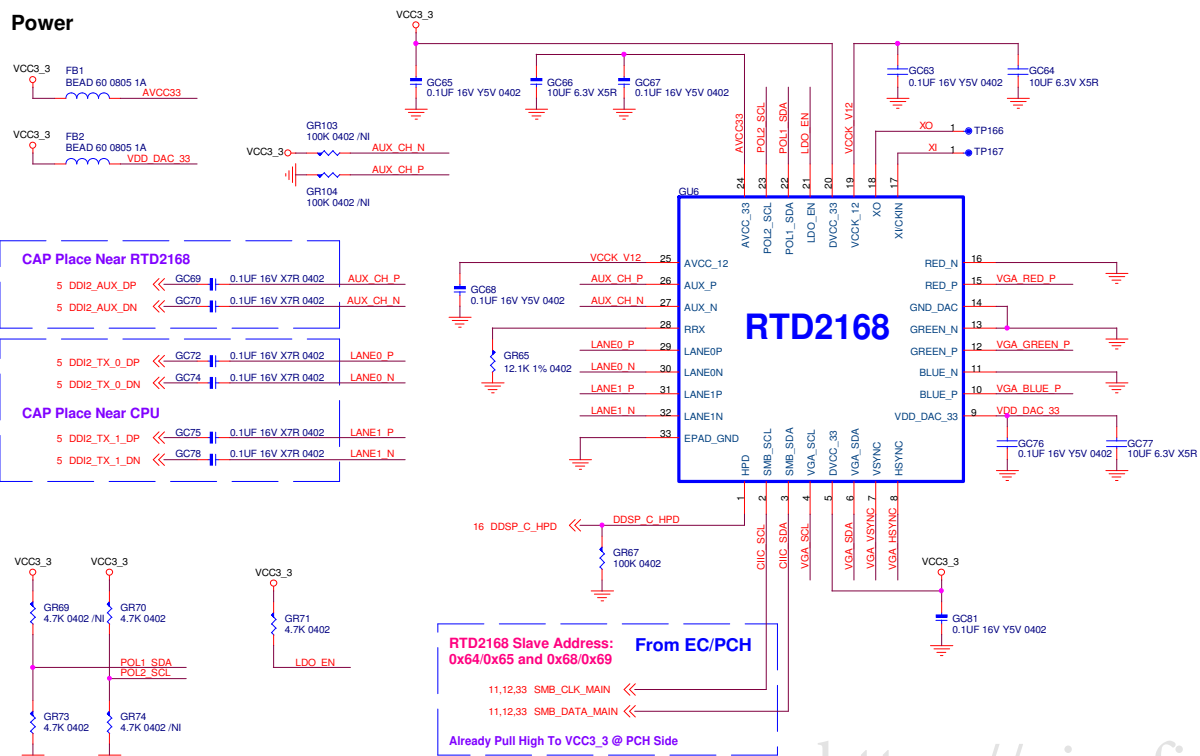
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Title	PCIEX16 SLOT 1 & 2
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Size C	Document Number IH11M-MHS
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Rev

Power



Mode Configure Table(Power On Latch)

		POL1_SDA(PIN22)	
		0	1
POL2_SCL(PIN23)	0	X	EP MODE
	1	ROM ONLY MODE	EPPROM MODE

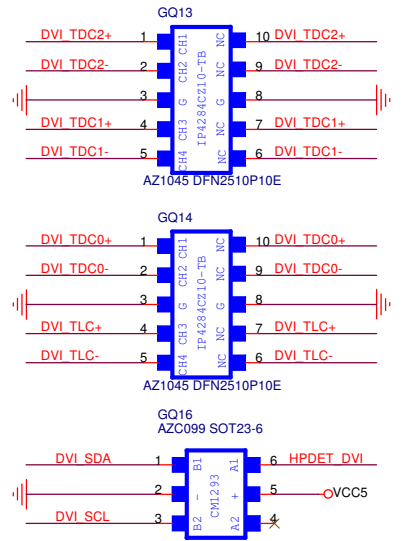
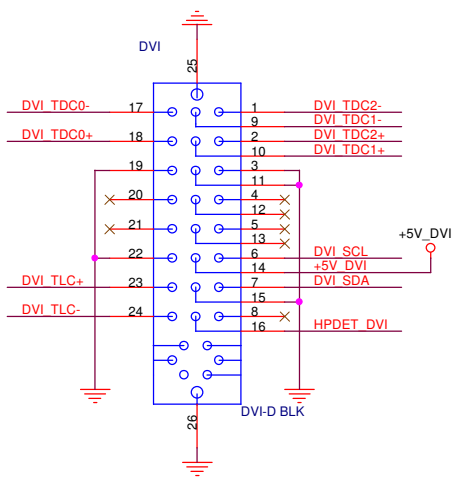
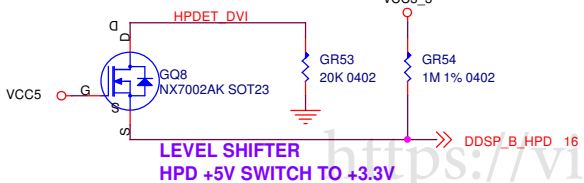
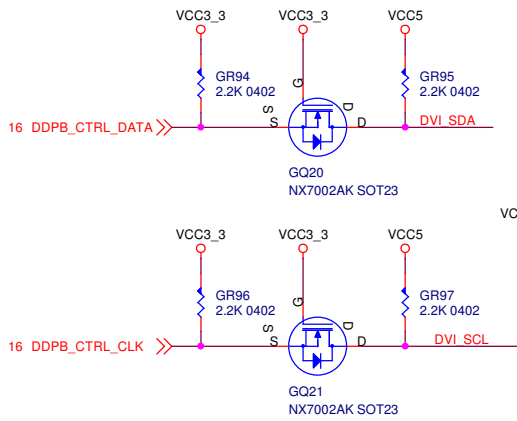
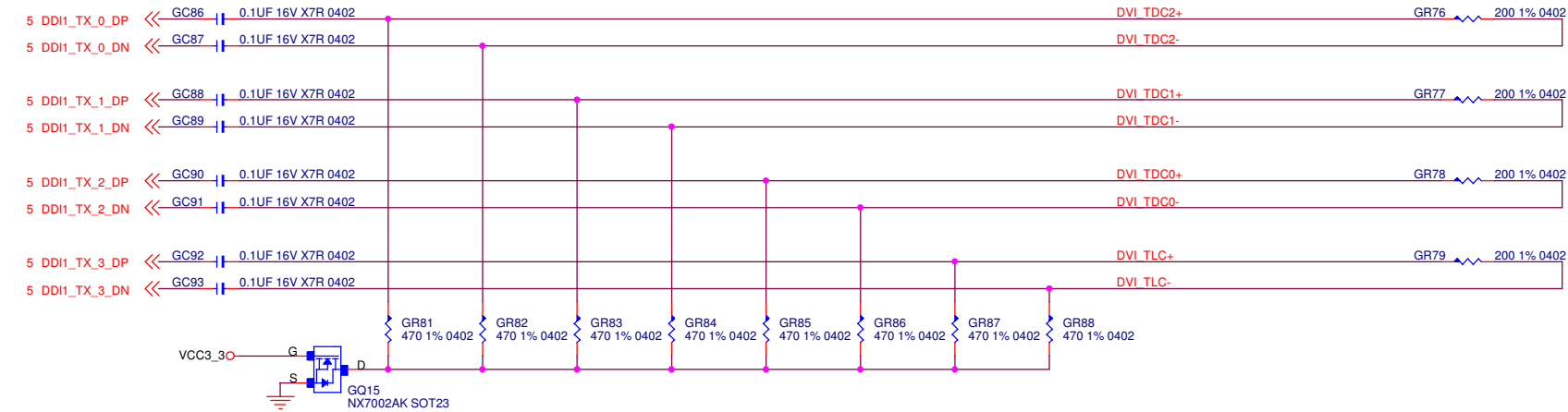
Embedded LDO

LDO_EN(PIN21)	
0	1
VCCK_V12 from External 1.2V	VCCK_V12 from Embedded LDO

Table 12 Power consumption by using embedded LDO and embedded clock source

Active Resolution / Standby	DP Config.	Min	Type	Max	Unit
1280x800x60(74.25-MHz)	1-Lane	-	400	450	mW
1600x900x60(103-MHz)	1-Lane	-	420	480	mW
1920x1080x60(148-MHz)	2-Lane	-	480	595	mW
Stand-by mode	-	-	7.5	8	mW

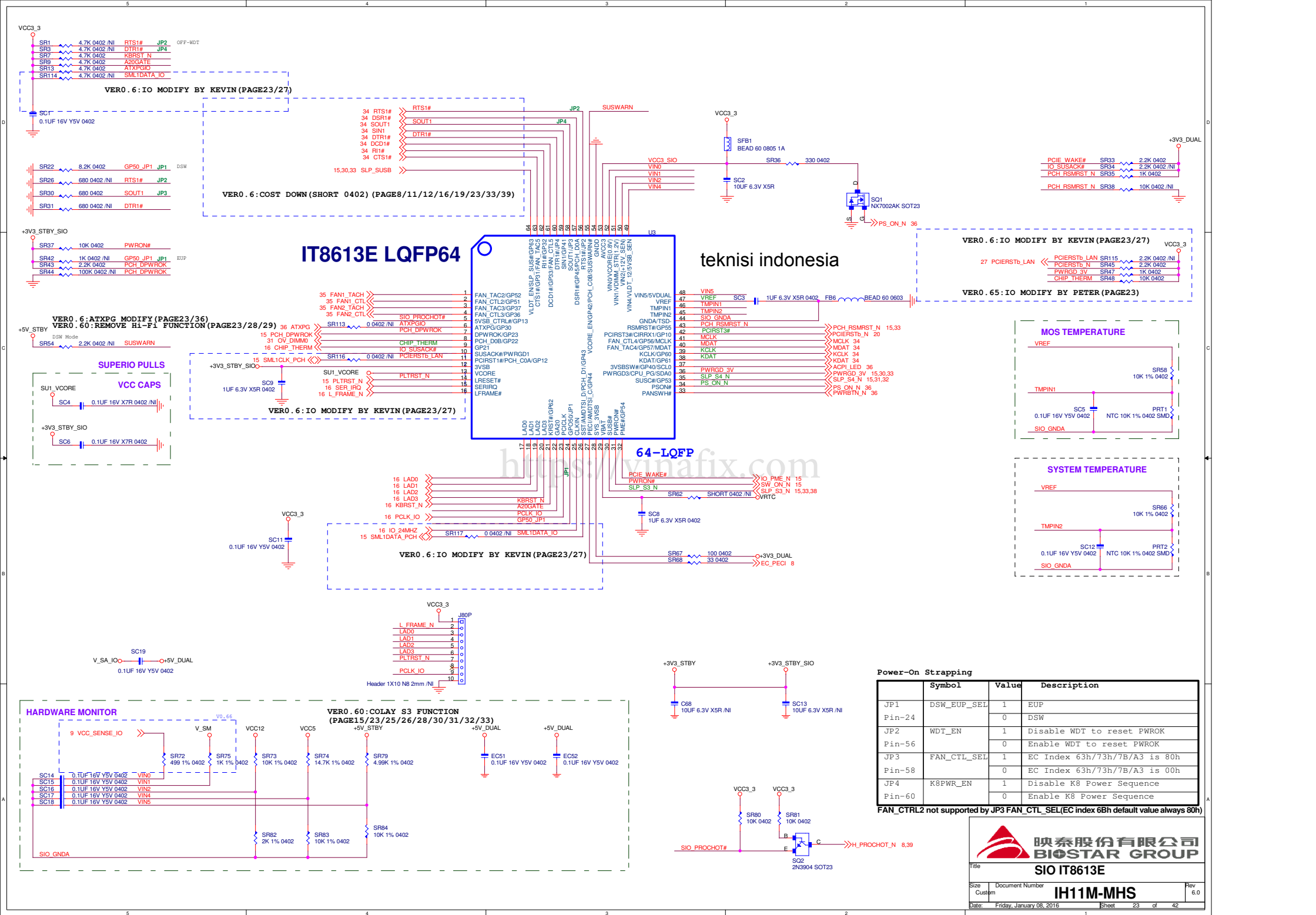


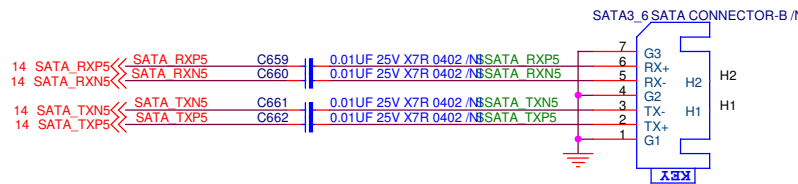
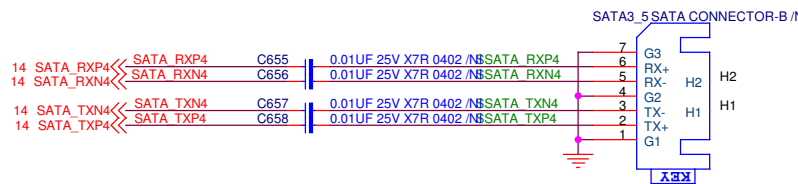
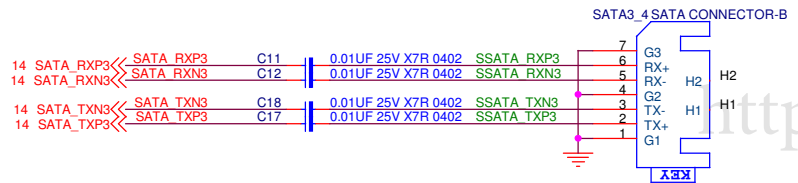
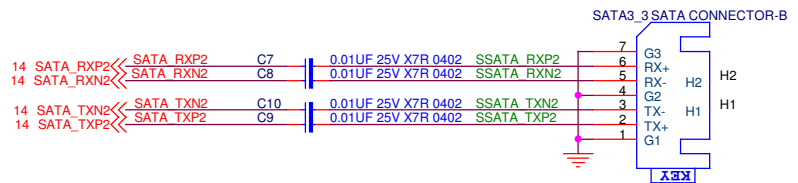
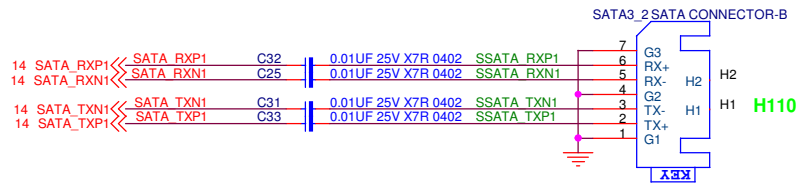
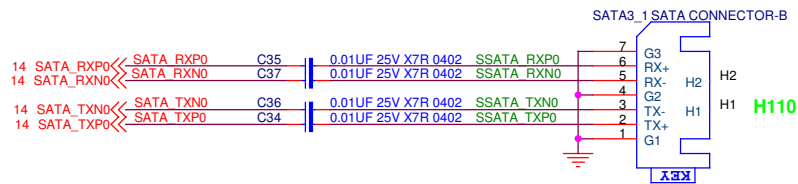


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Title DVI-I CONNECTOR		
Size B	Document Number IH11M-MHS	Rev 6.0
Date Friday, January 08, 2016	Sheet 22	of 42



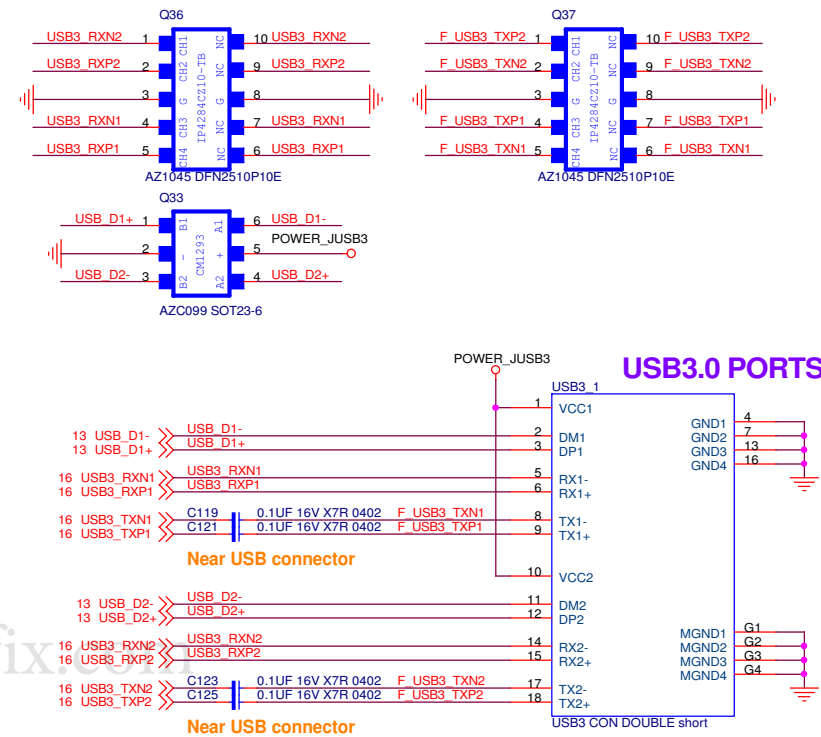


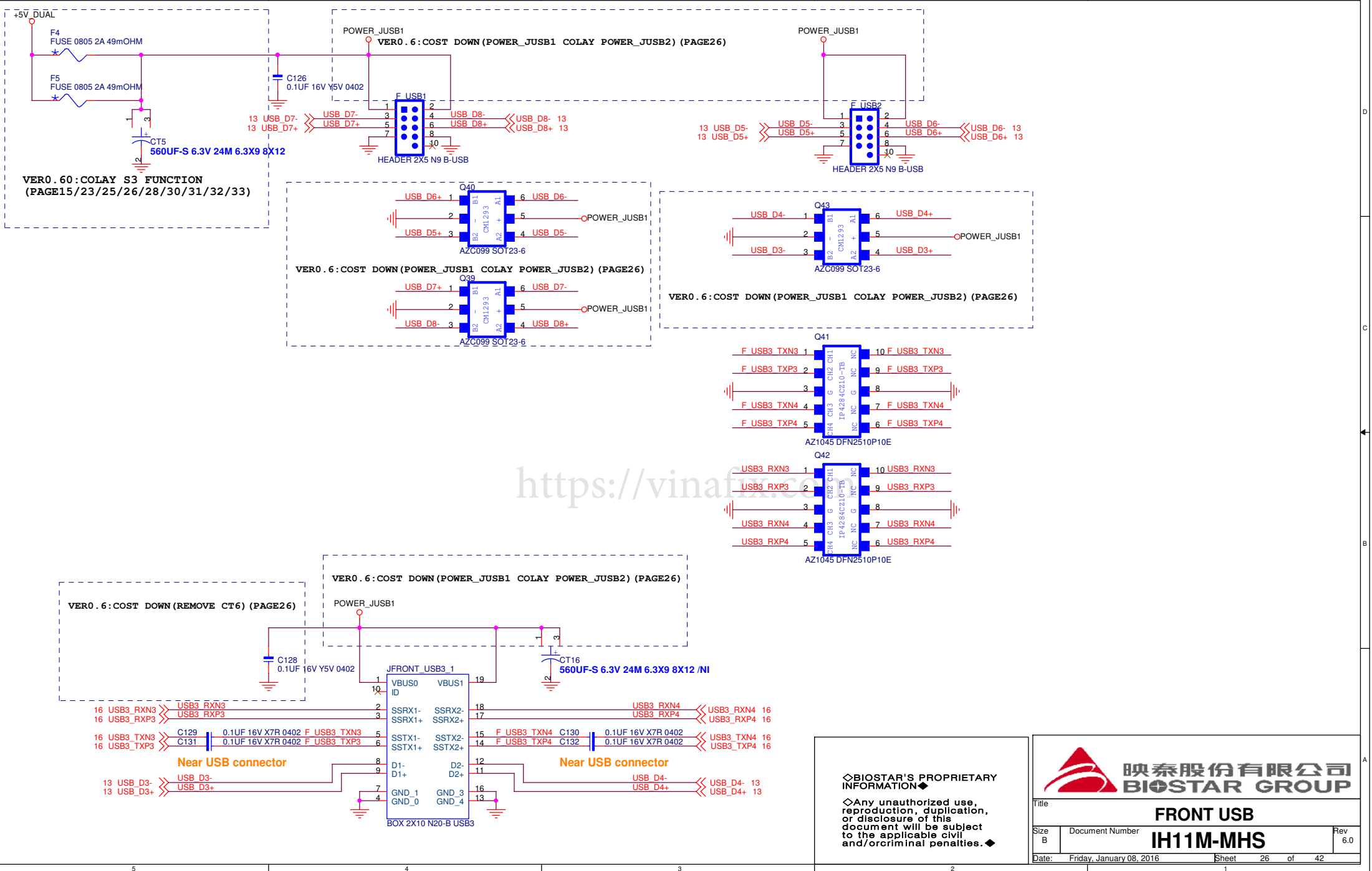
VER0.65:NEW ADD SATA CONN (PAGE14/24)

VER0.60:REMOVE SATA EXPRESS CONN (PAGE14/16/17/24)

<https://vinafix.com>

Title SATA EXPRESS			
Size B	Document Number	IH11M-MHS	
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		Rev	6.0






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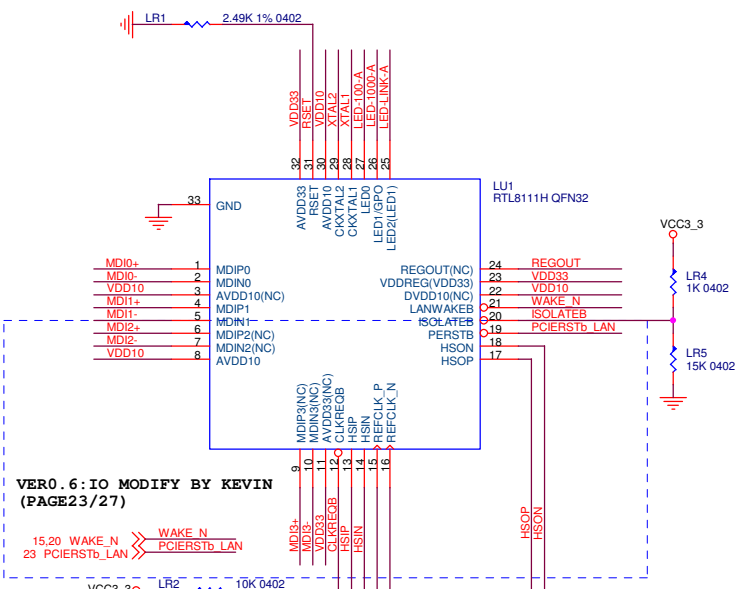


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Title: FRONT USB

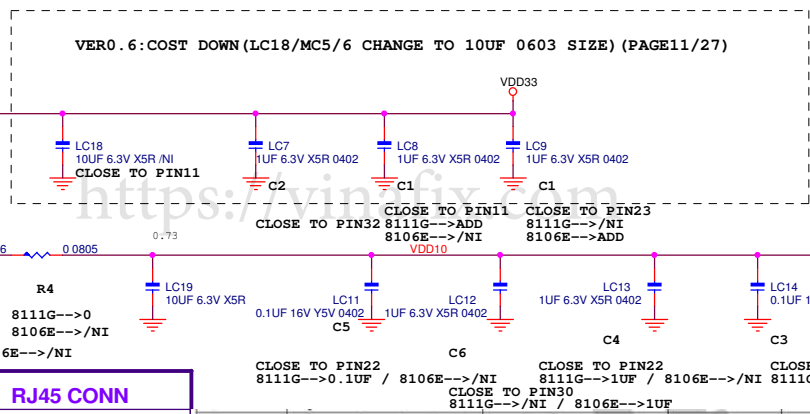
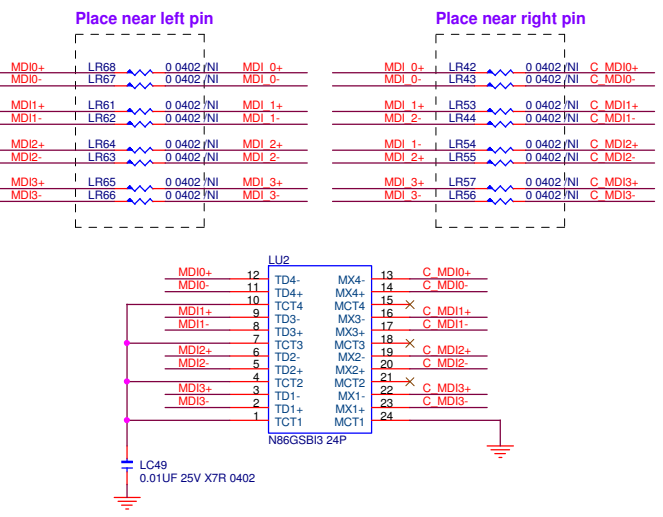
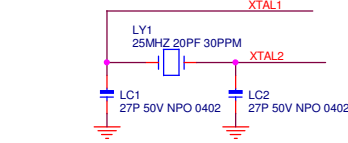
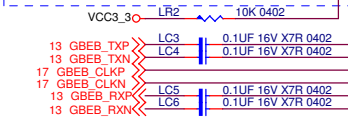
Size: B Document Number: IH11M-MHS Rev: 6.0

Date: Friday, January 08, 2016 Sheet: 26 of 42



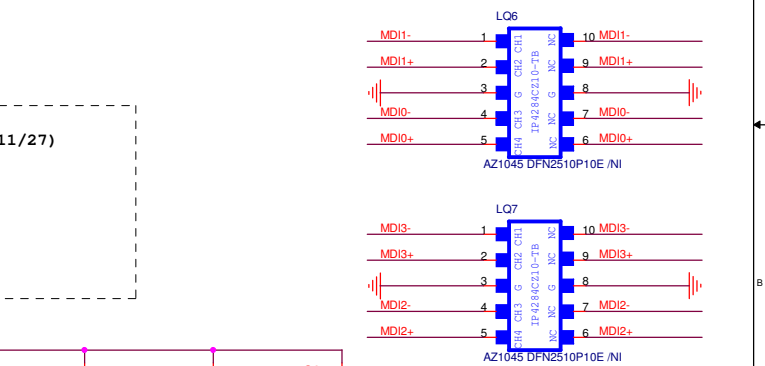
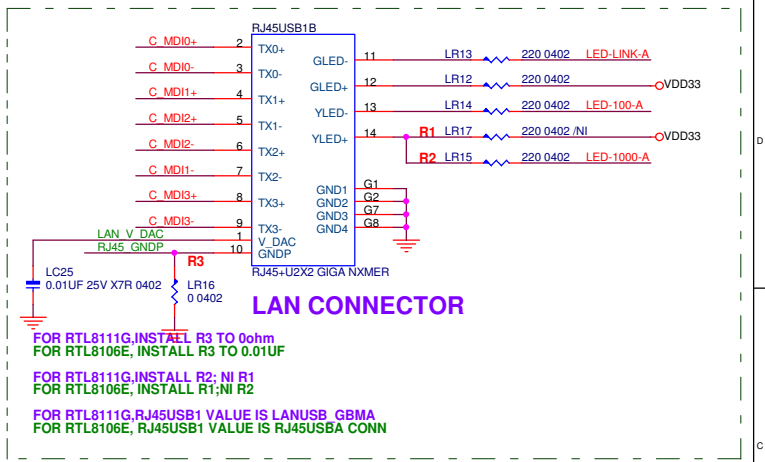
VER0.6:IO MODIFY BY KEVIN
(PAGE23/27)

15.20 WAKE_N WAKE_N
23 PCIERSTb_LAN PCIERSTb_LAN



LAN PARTS	R1	R2	R3	R4	C1	C2	C3	C4	C5	C6	RJ45 CONN
RTL8111H	X	O	0ohm	O	O	O	O	O	O	X	LANUSB_GBMA
RTL8107E	X	O	0.01uF	O						O	RJ45USBA CONN

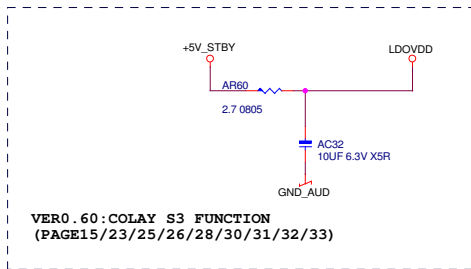
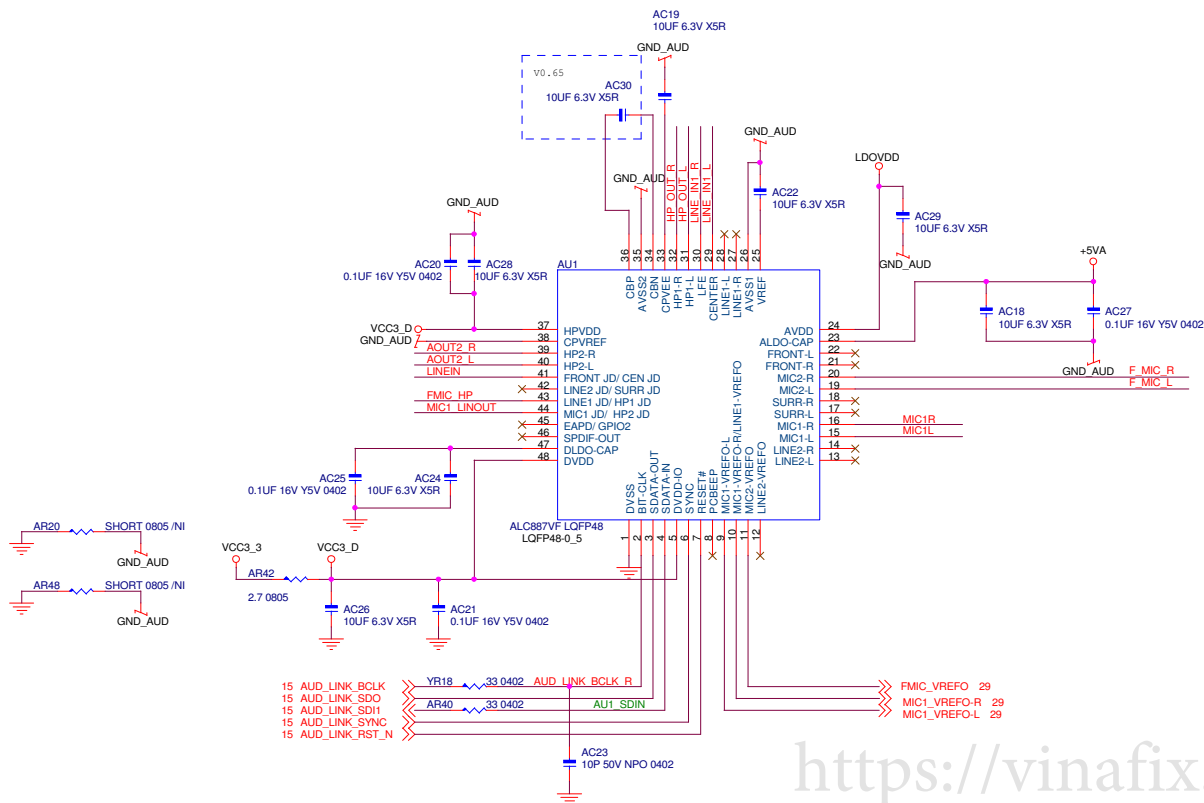
LAN PARTS	R1	R2	R3	R4	C1	C2	C3	C4	C5	C6	RJ45 CONN
RTL8111G	X	O	0ohm	O	O	O	O	O	O	X	LANUSB_GBMA
RTL8106E	O	X	0.01uF	X	X	X	X	X	X	O	RJ45USBA CONN



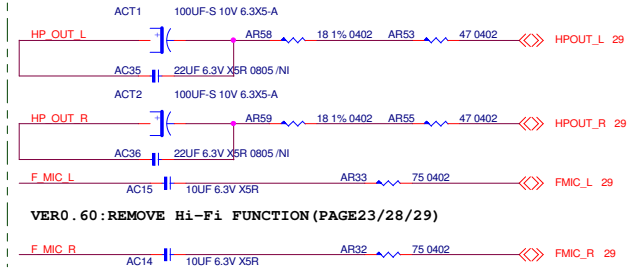
RTL8111H/8107E

IH11M-MHS

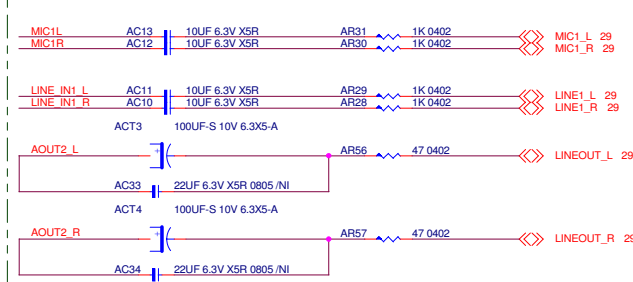
Date: Friday, January 08, 2016 Sheet 27 of 42



FRONT CHANNEL

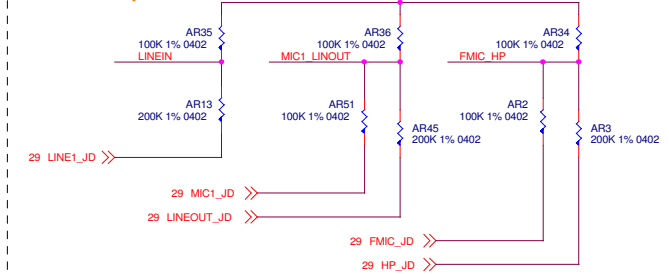


REAR CHANNEL



JD Group

as close as possible to AU1



Vinafix.com

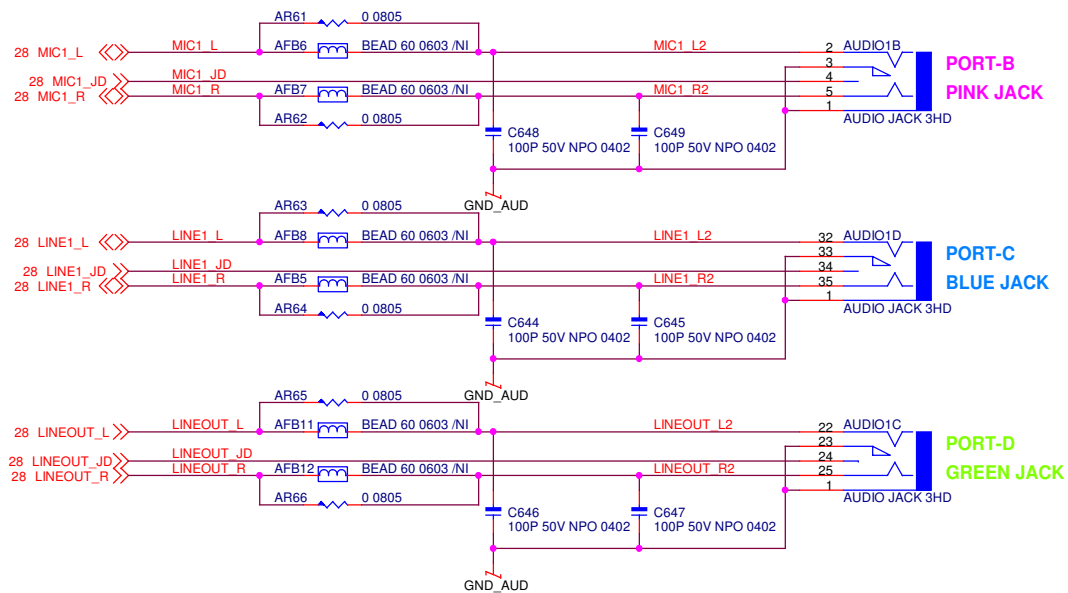
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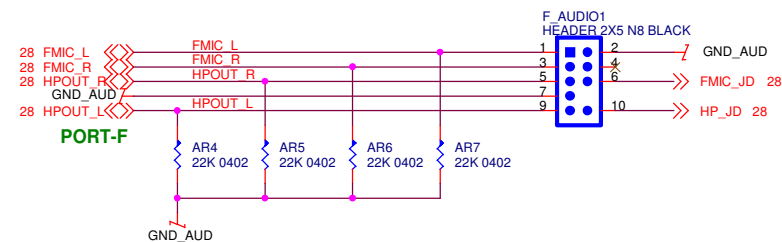
Title: **AUDIO CODEC ALC887**

Size: Custom Document Number: **IH11M-MHS** Rev: 6.0

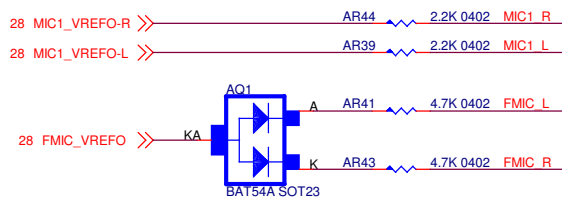
Date: Friday, January 08, 2016 Sheet: 28 of 42



FRONT AUDIO HEADER



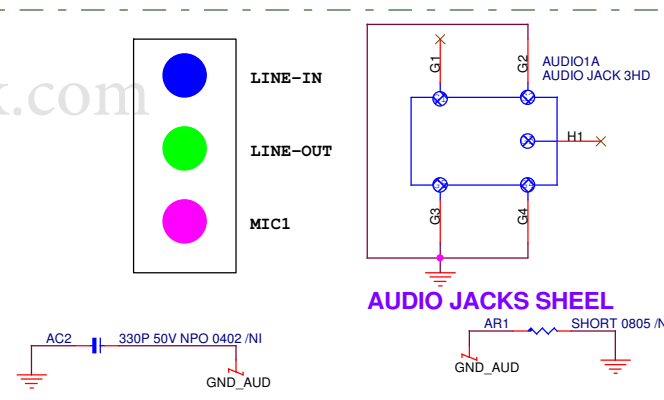
MIC VREF



SPDIF CONNECTOR

V0.66

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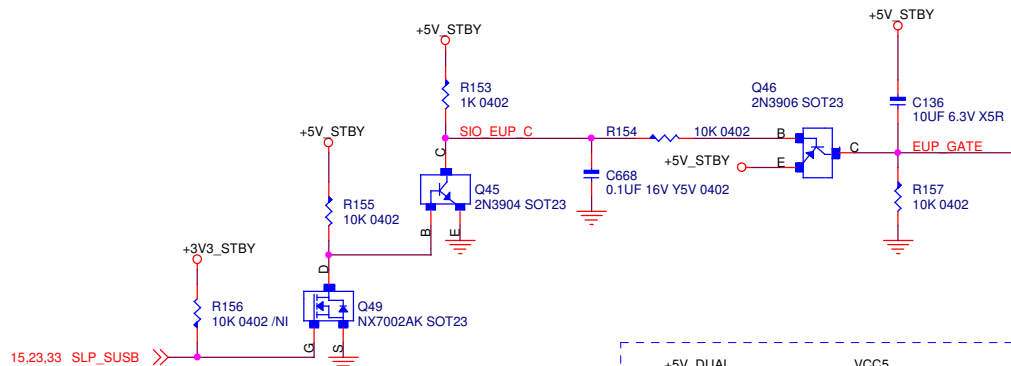


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Title
AUDIO CONNECTOR

Size B Document Number **IH11M-MHS** Rev 6.0

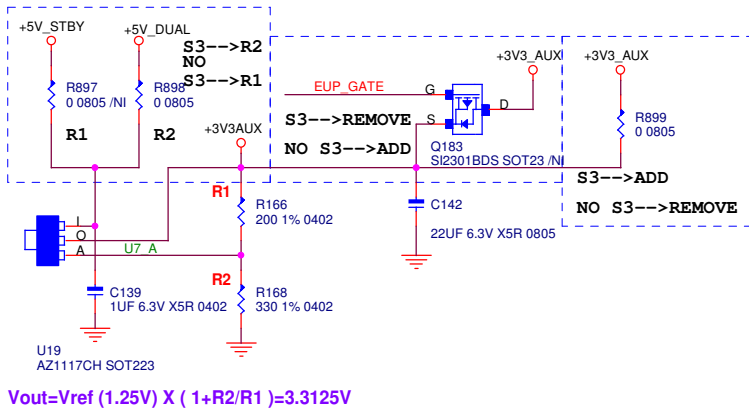
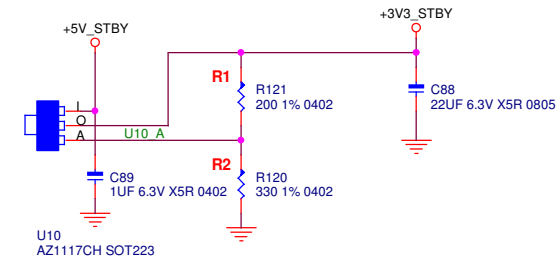
Date: Friday, January 08, 2016 Sheet 29 of 42



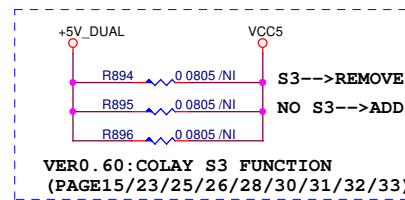
Energy-Using Product(EUP)

SLP_SUSB Hight :EUP OFF
SLP_SUSB Low :EUP ON

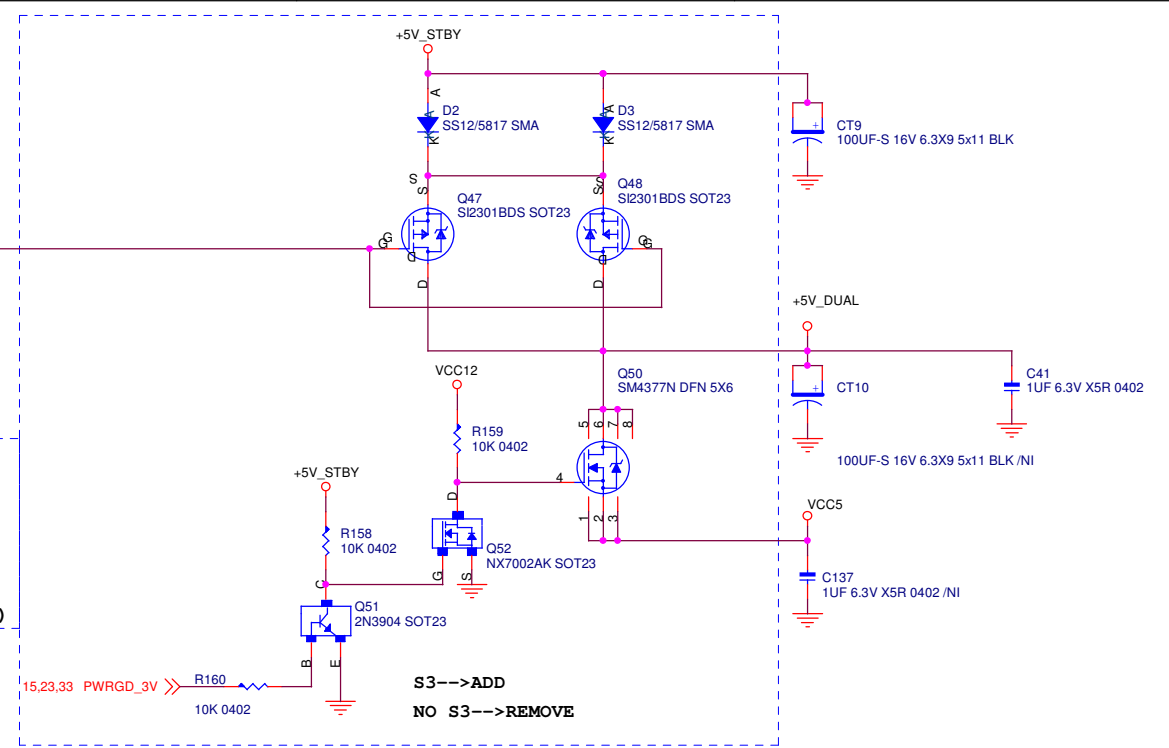
$$V_{out} = V_{ref} (1.25V) \times (1 + R_2/R_1) = 3.3125V$$



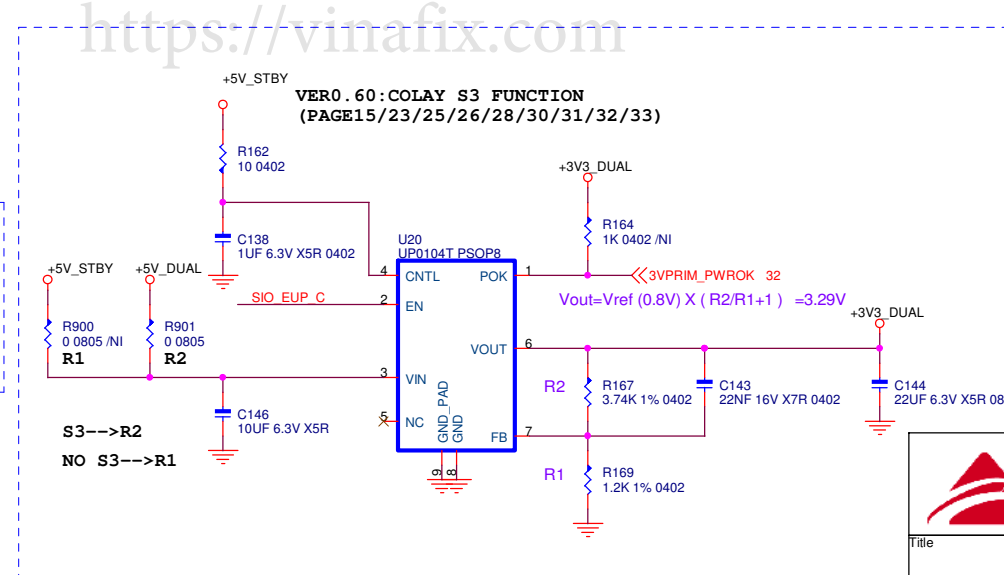
$$V_{out} = V_{ref} (1.25V) \times (1 + R_2/R_1) = 3.3125V$$



VERO.60:COLAY S3 FUNCTION
(PAGE15/23/25/26/28/30/31/32/33)



S3-->ADD
NO S3-->REMOVE



VERO.60:COLAY S3 FUNCTION
(PAGE15/23/25/26/28/30/31/32/33)

S3-->R2
NO S3-->R1

$$V_{out} = V_{ref} (0.8V) \times (R_2/R_1 + 1) = 3.29V$$

VER0.60:COLAY S3 FUNCTION
(PAGE15/23/25/26/28/30/31/32/33)



OV_VSM	OV_DIMM0
Default 1.213V	1
1.36V	0

VER0.6:COST DOWN(MCT2/3/CT11 CHANGE TO 560UF) (PAGE31/32)



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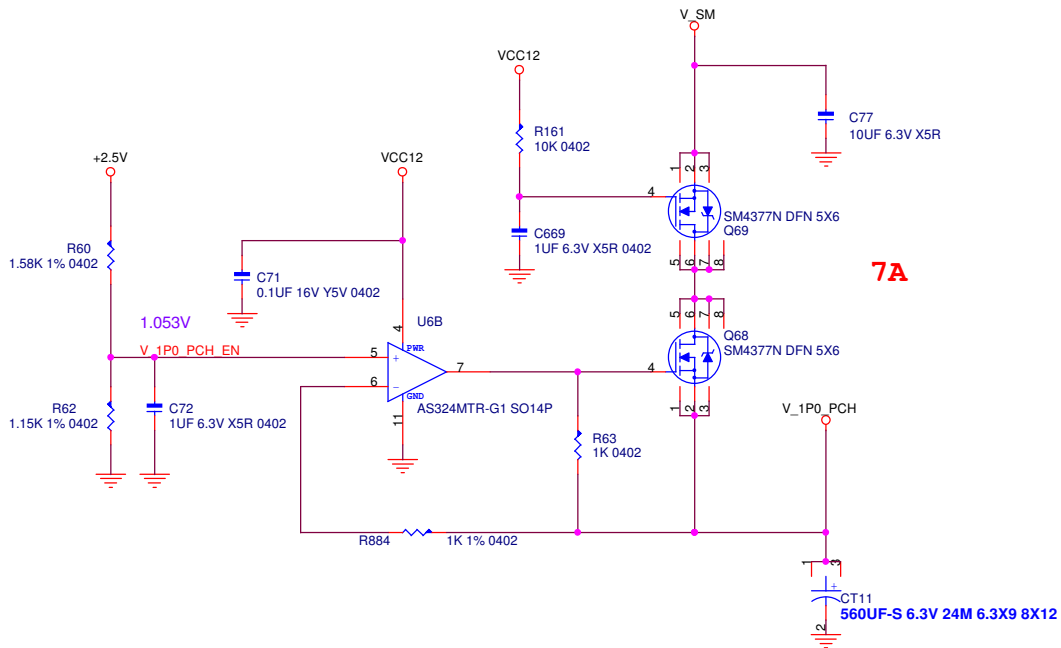


MEMORY DC-DC

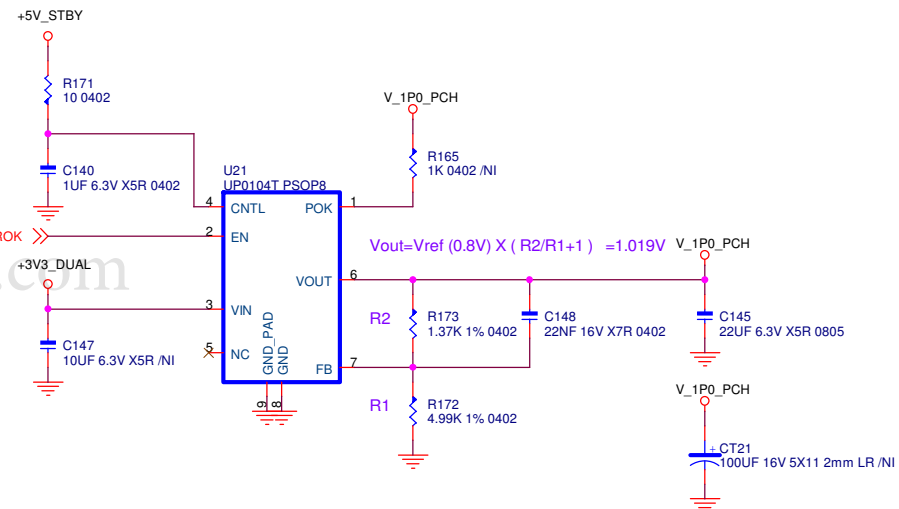
Size C	Document Number IH11M-MHS	Rev 6.0
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Date: Friday, January 08, 2016

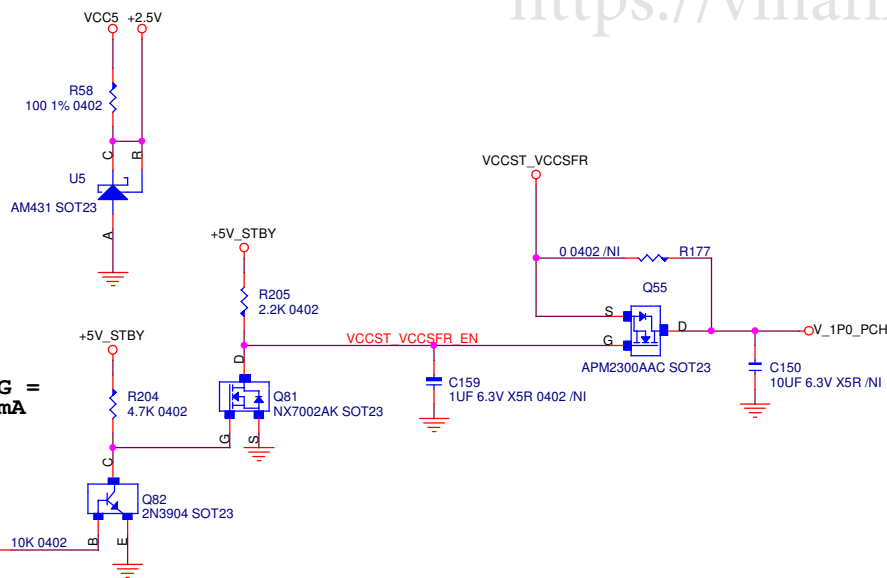
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7A




$$V_{out} = V_{ref} (0.8V) \times (R2/R1 + 1) = 1.019V$$



$$VCCST+VCCSTG = 0.06+0.06 \text{ mA}$$

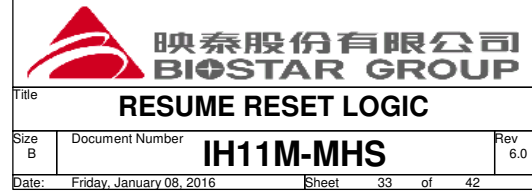
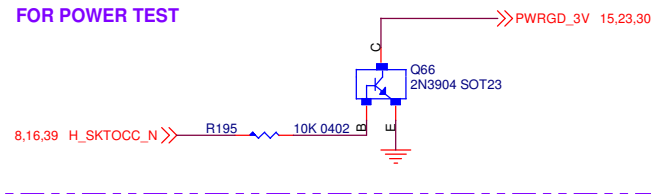
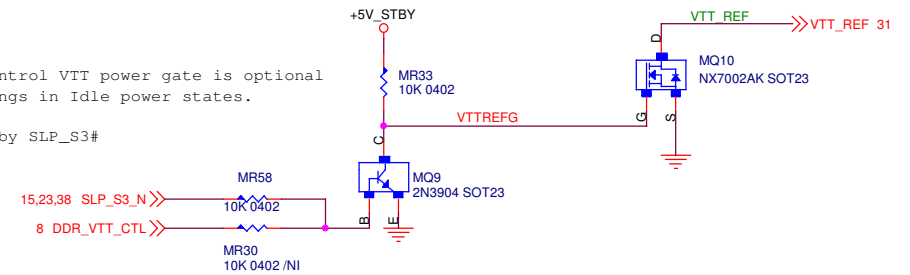
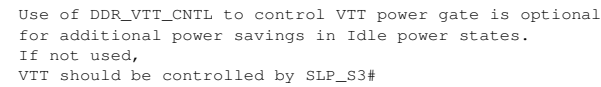
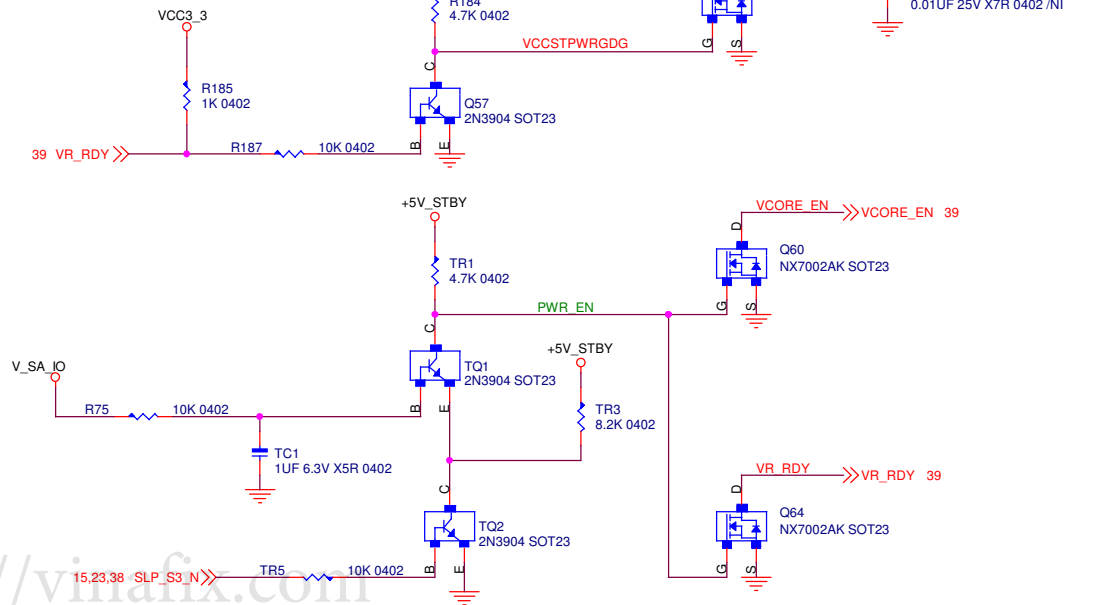
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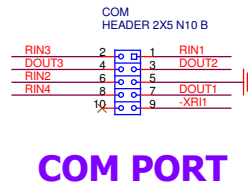
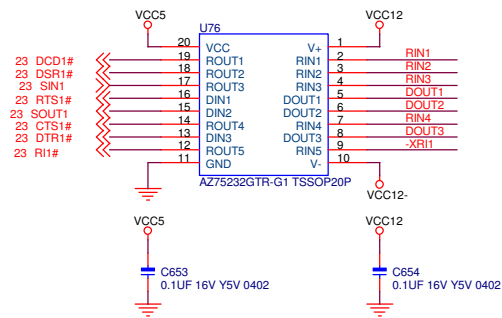
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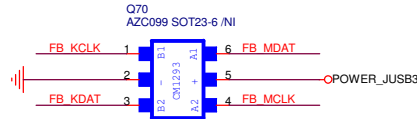
Title V_1P0_PCH		
Size B	Document Number IH11M-MHS	Rev 6.0
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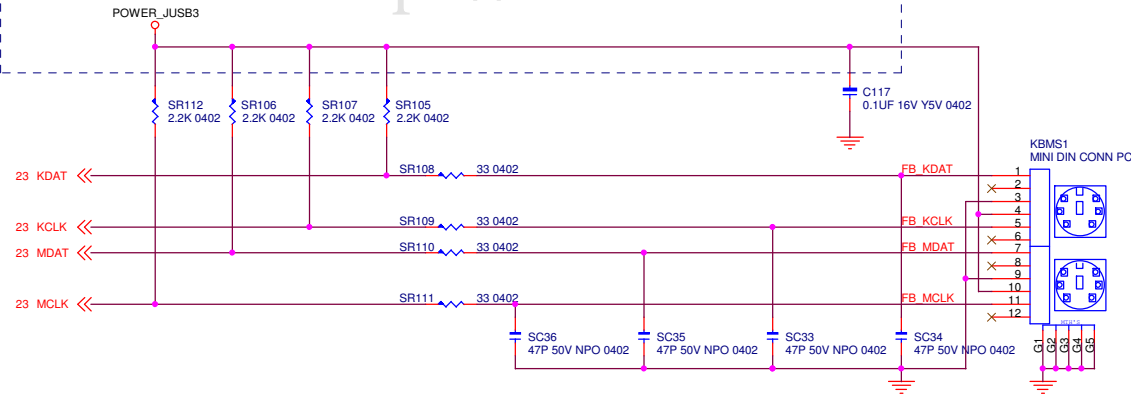
COM PORT

WAKE ON RING



KEYBOARD & MOUSE

VER0.6: COST DOWN (POWER_JUSB4/POWER_JUSB5 COLAY) (PAGE25/34)

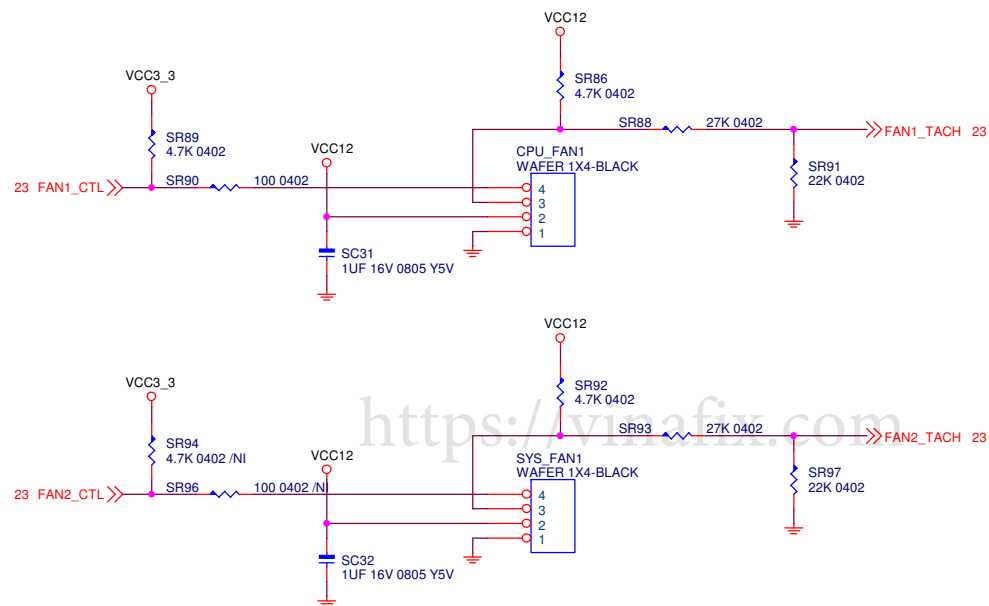


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File: **COM1 / PS2 CONN**

Size: Custom	Document Number: IH11M-MHS	Rev: 6.0
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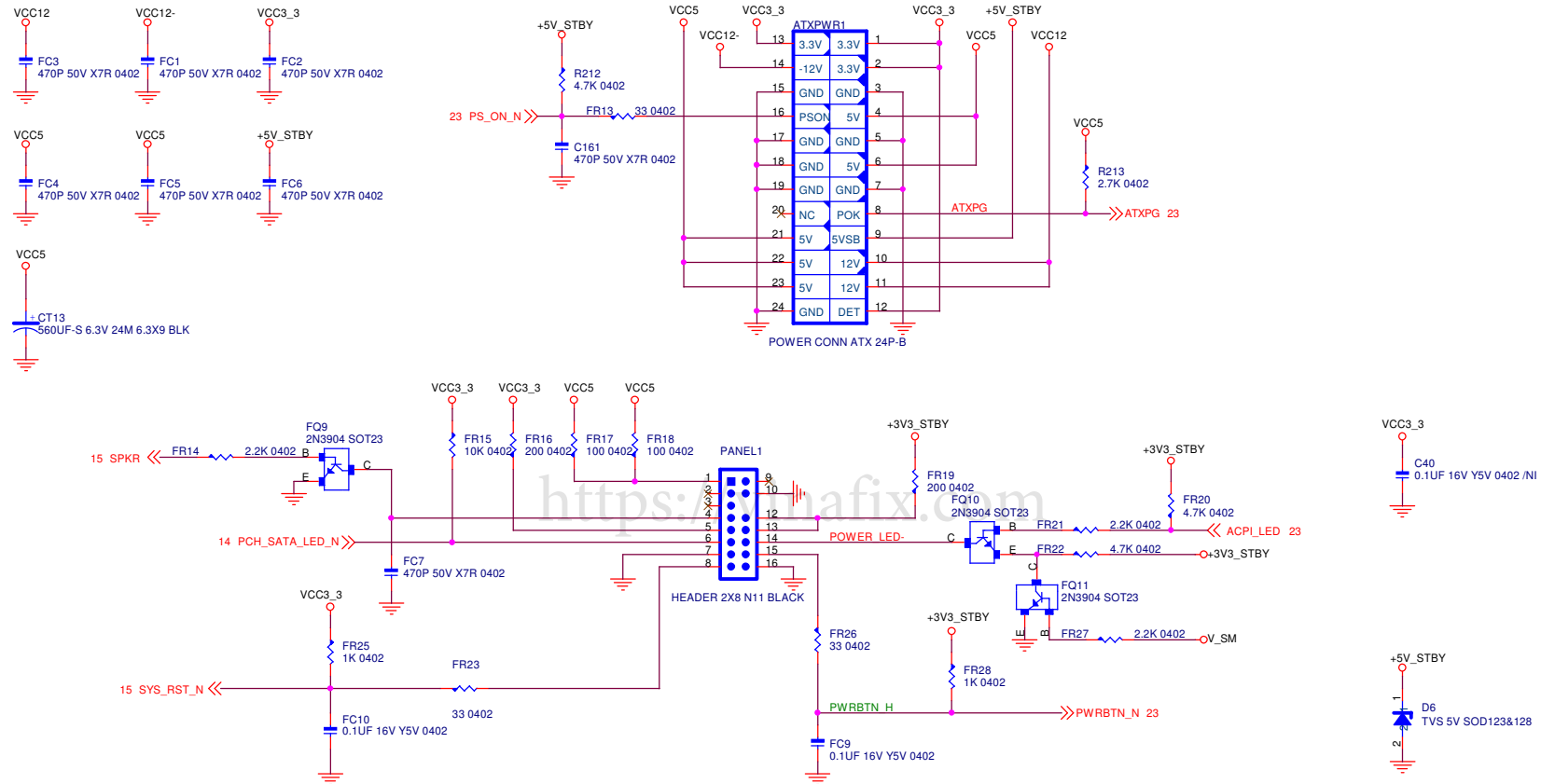
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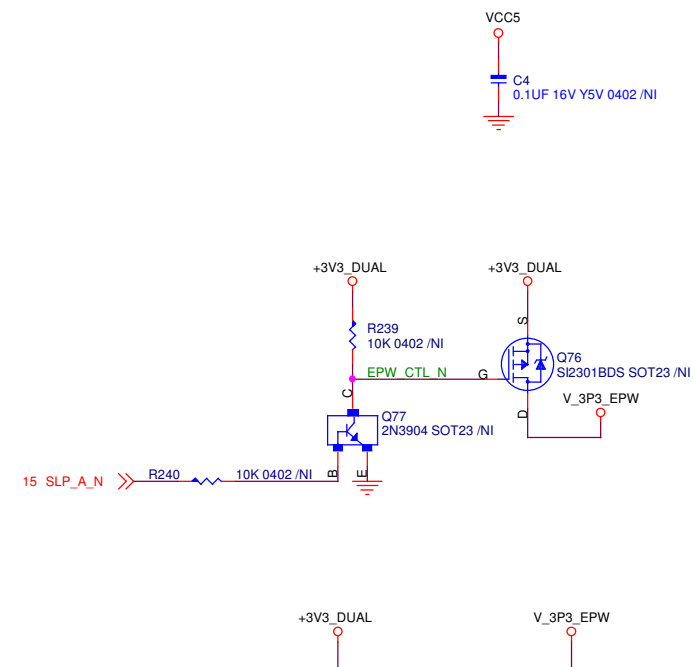
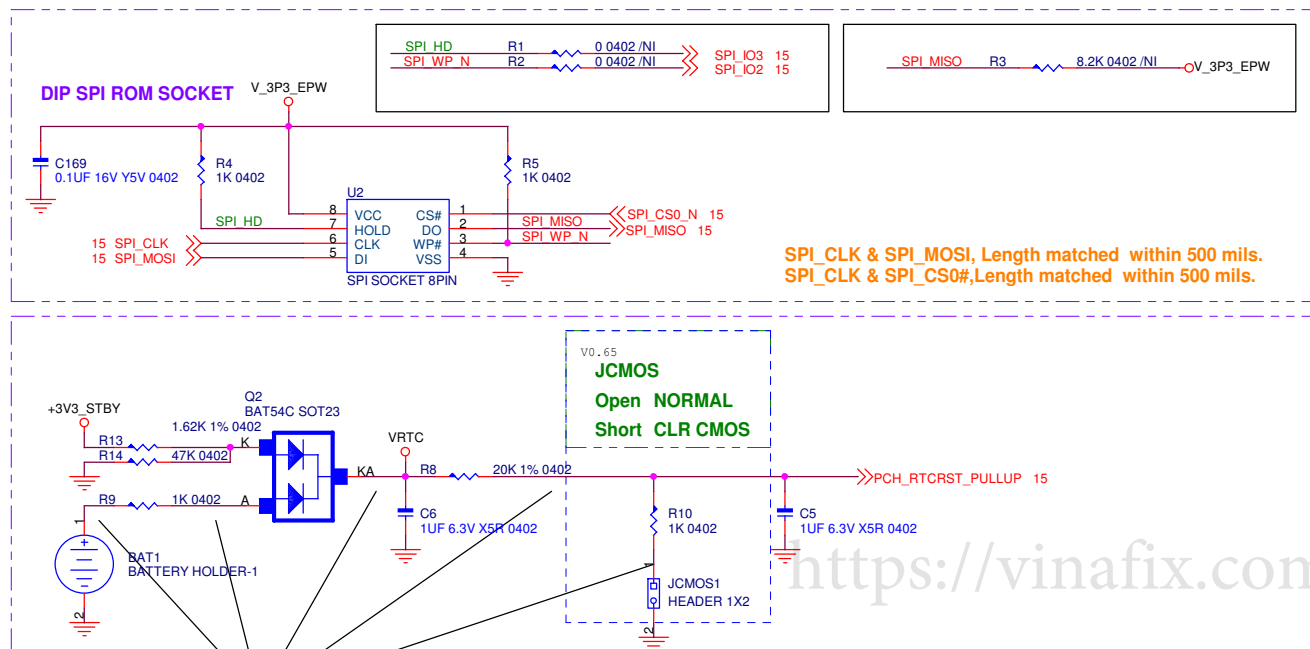
Title			FAN & PS2		
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FP PART: F+Reference



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Title 24PIN CONN & FP	
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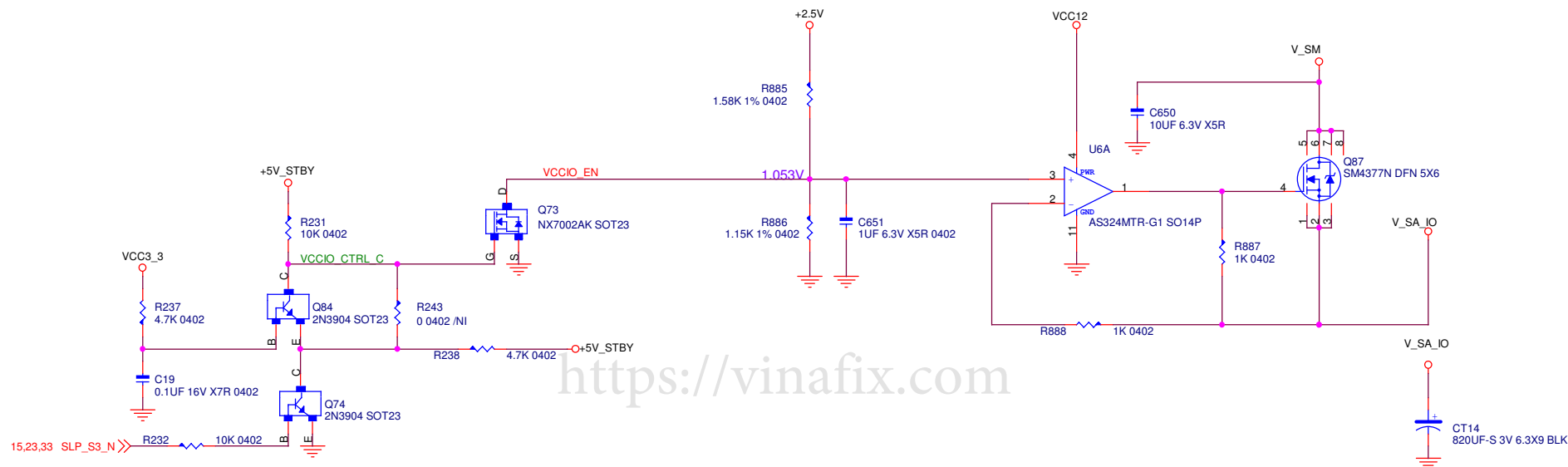
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Title			SPI ROM/RTC CRYSTAL/BAT
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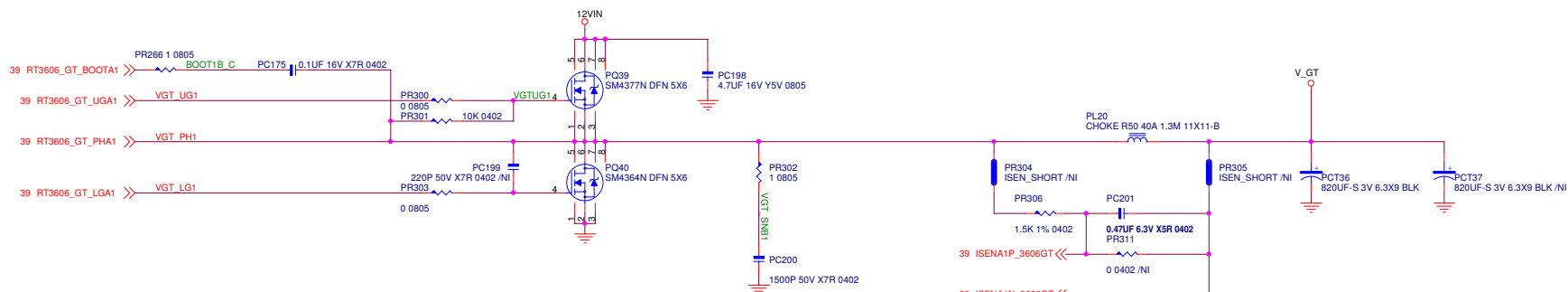


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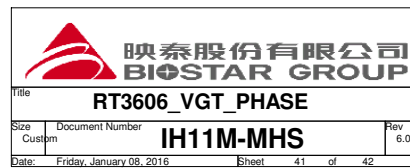
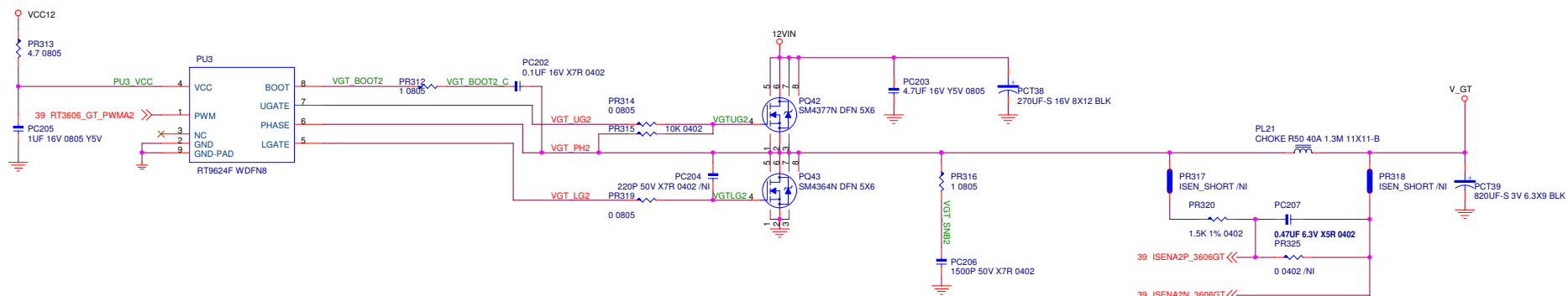


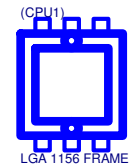
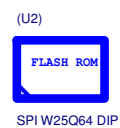
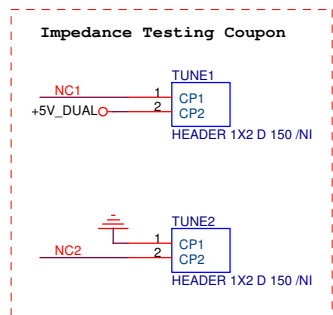
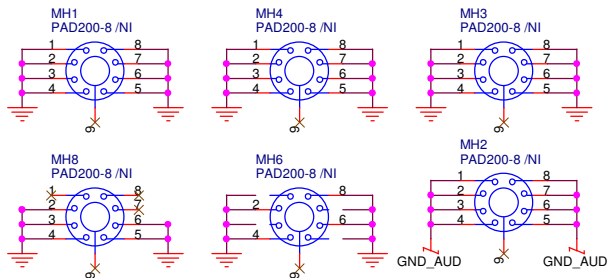
Title			VCCIO/VCCSA DC-DC		
Size	Document Number	IH11M-MHS			Rev
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Skylake S-line 42 95W RT3606_VGT



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